Data sheet acquired from Harris Semiconductor
SCHS046I

August 1998 - Revised May 2004

CMOS Hex Buffer/Converters

The CD4049UB and CD4050B devices are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC} = 5V, $V_{OL} \leq$ 0.4V, and $I_{OL} \geq$ 3.3mA.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

Features

- CD4049UB Inverting
- CD4050B Non-Inverting
- High Sink Current for Driving 2 TTL Loads
- High-To-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1µA at 18V Over Full Package Temperature Range; 100nA at 18V and 25^{o}C
- 5V, 10V and 15V Parametric Ratings

Applications

- CMOS to DTL/TTL Hex Converter
- CMOS Current “Sink” or “Source” Driver
- CMOS High-To-Low Logic Level Converter

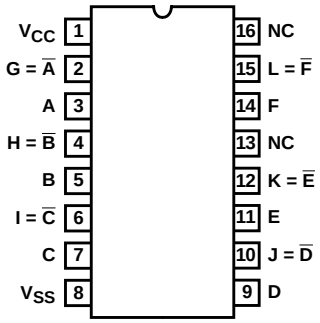
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD4049UBF3A	-55 to 125	16 Ld CERDIP
CD4050BF3A	-55 to 125	16 Ld CERDIP
CD4049UBD	-55 to 125	16 Ld SOIC
CD4049UBDR	-55 to 125	16 Ld SOIC
CD4049UBDT	-55 to 125	16 Ld SOIC
CD4049UBDW	-55 to 125	16 Ld SOIC
CD4049UBDWR	-55 to 125	16 Ld SOIC
CD4049UBE	-55 to 125	16 Ld PDIP
CD4049UBNSR	-55 to 125	16 Ld SOP
CD4049UBPW	-55 to 125	16 Ld TSSOP
CD4049UBPWR	-55 to 125	16 Ld TSSOP
CD4050BD	-55 to 125	16 Ld SOIC
CD4050BDR	-55 to 125	16 Ld SOIC
CD4050UBDT	-55 to 125	16 Ld SOIC
CD4050BDW	-55 to 125	16 Ld SOIC
CD4050BDWR	-55 to 125	16 Ld SOIC
CD4050BE	-55 to 125	16 Ld PDIP
CD4050NSR	-55 to 125	16 Ld SOP
CD4050BPW	-55 to 125	16 Ld TSSOP
CD4050BPWR	-55 to 125	16 Ld TSSOP

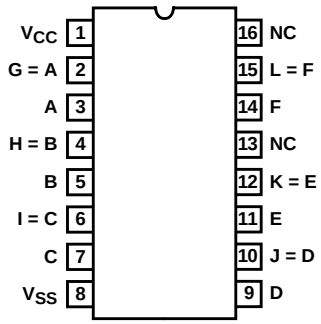
NOTE: When ordering, use the entire part number. The suffix R denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinouts

CD4049UB (PDIP, CERDIP, SOIC, SOP, TSSOP)
TOP VIEW



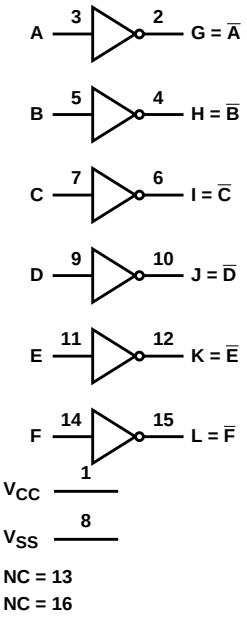
CD4050B (PDIP, CERDIP, SOIC, SOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

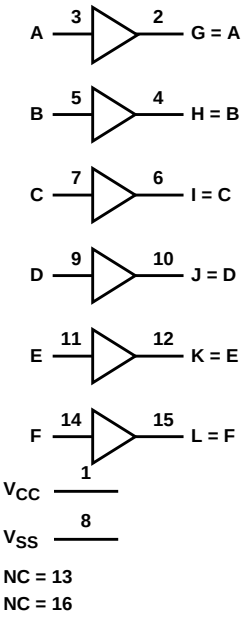
Functional Block Diagrams

CD4049UB



NC = 13
NC = 16

CD4050B



NC = 13
NC = 16

Schematic Diagrams

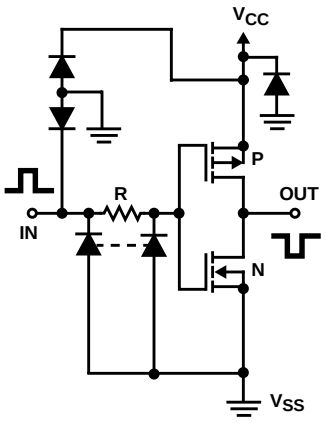


FIGURE 1A. SCHEMATIC DIAGRAM OF CD4049UB, 1 OF 6 IDENTICAL UNITS

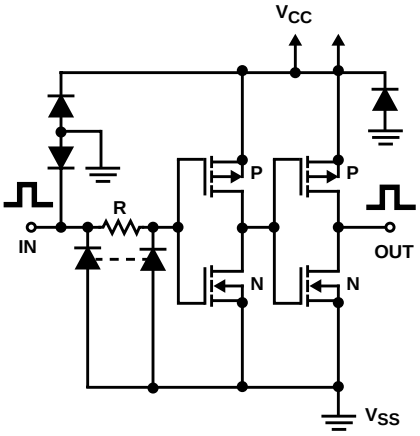


FIGURE 1B. SCHEMATIC DIAGRAM OF CD4050B, 1 OF 6 IDENTICAL UNITS

Absolute Maximum Ratings

Supply Voltage (V+ to V-) . . . . . -0.5V to 20V
DC Input Current, Any One Input . . . . . ±10mA

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note1):
E (PDIP) Package . . . . . $67^oC/W$
D (SOIC) Package . . . . . $73^oC/W$
DW (SOIC) Package . . . . . $57^oC/W$
NS (SOP) Package . . . . . $64^oC/W$
PW (TSSOP) Package . . . . . $108^oC/W$
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . 65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 265^oC
SOIC - Lead Tips Only

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (^oC)							UNITS
								25			
	V_O (V)	V_{IN} (V)	V_{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Quiescent Device Current I_{DD} (Max)	-	0,5	5	1	1	30	30	-	0.02	1	µA
	-	0,10	10	2	2	60	60	-	0.02	2	µA
	-	0,15	15	4	4	120	120	-	0.02	4	µA
	-	0,20	20	20	20	600	600	-	0.04	20	µA
Output Low (Sink) Current I_{OL} (Min)	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	-	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	-	mA
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	-	mA
	1.5	0,15	15	26	25	20	18	24	48	-	mA
Output High (Source) Current I_{OH} (Min)	4.6	0,5	5	-0.81	-0.73	-0.58	-0.48	-0.65	-1.2	-	mA
	2.5	0,5	5	-2.6	-2.4	-1.9	-1.55	-2.1	-3.9	-	mA
	9.5	0,10	10	-2.0	-1.8	-1.35	-1.18	-1.65	-3.0	-	mA
	13.5	0,15	15	-5.2	-4.8	-3.5	-3.1	-4.3	-8.0	-	mA
Out Voltage Low Level V_{OL} (Max)	-	0,5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0,15	15	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage High Level V_{OH} (Min)	-	0,5	5	4.95	4.95	4.95	4.95	4.95	5	-	V
	-	0,10	10	9.95	9.95	9.95	9.95	9.95	10	-	V
	-	0,15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage, V_{IL} (Max) CD4049UB	4.5	-	5	1	1	1	1	-	-	1	V
	9	-	10	2	2	2	2	-	-	2	V
	13.5	-	15	2.5	2.5	2.5	2.5	-	-	2.5	V
Input Low Voltage, V_{IL} (Max) CD4050B	0.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1	-	10	3	3	3	3	-	-	3	V
	1.5	-	15	4	4	4	4	-	-	4	V

DC Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (^oC)							UNITS
								25			
	V_O (V)	V_{IN} (V)	V_{CC} (V)	-55	-40	85	125	MIN	TYP	MAX	
Input High Voltage, V_{IH} Min CD4049UB	0.5	-	5	4	4	4	4	4	-	-	V
	1	-	10	8	8	8	8	8	-	-	V
	1.5	-	15	12.5	12.5	12.5	12.5	12.5	-	-	V
Input High Voltage, V_{IH} Min CD4050B	4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	9	-	10	7	7	7	7	7	-	-	V
	13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I_{IN} Max	-	0,18	18	±0.1	±0.1	±1	±1	-	$\pm10^{-5}$	±0.1	µA

AC Electrical Specifications

$T_A = 25^oC$, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ

PARAMETER	TEST CONDITIONS		LIMITS (ALL PACKAGES)		UNITS
	V_{IN}	V_{CC}	TYP	MAX	
Propagation Delay Time Low to High, t_{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	ns
	10	5	45	90	ns
	15	15	25	50	ns
	15	5	45	90	ns
Propagation Delay Time Low to High, t_{PLH} CD4050B	5	5	70	140	ns
	10	10	40	80	ns
	10	5	45	90	ns
	15	15	30	60	ns
	15	5	40	80	ns
Propagation Delay Time High to Low, t_{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	ns
	10	5	15	30	ns
	15	15	15	30	ns
	15	5	10	20	ns
Propagation Delay Time High to Low, t_{PHL} CD4050B	5	5	55	110	ns
	10	10	22	55	ns
	10	5	50	100	ns
	15	15	15	30	ns
	15	5	50	100	ns
Transition Time, Low to High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	ns
	15	15	30	60	ns
Transition Time, High to Low, t_{THL}	5	5	30	60	ns
	10	10	20	40	ns
	15	15	15	30	ns

AC Electrical Specifications $T_A = 25^oC$, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ **(Continued)**

PARAMETER	TEST CONDITIONS		LIMITS (ALL PACKAGES)		UNITS
	V_{IN}	V_{CC}	TYP	MAX	
Input Capacitance, C_{IN} CD4049UB	-	-	15	22.5	pF
Input Capacitance, C_{IN} CD4050B	-	-	5	7.5	pF

Typical Performance Curves

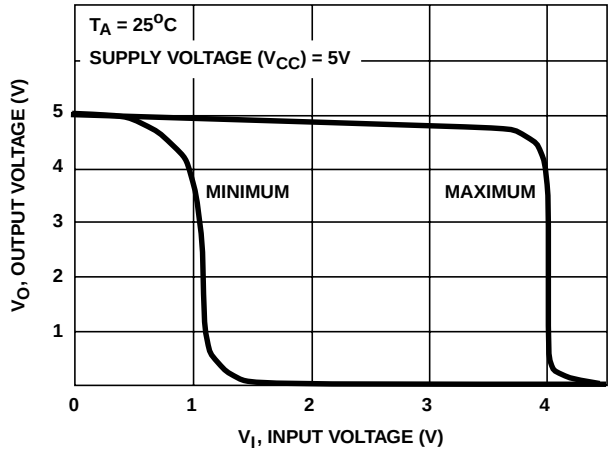


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4049UB

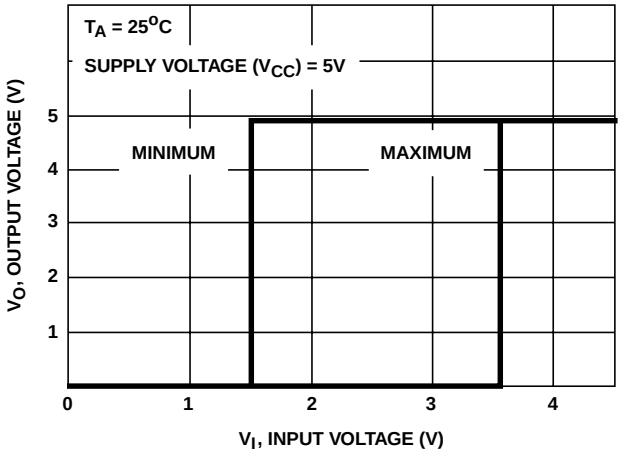


FIGURE 3. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4050B

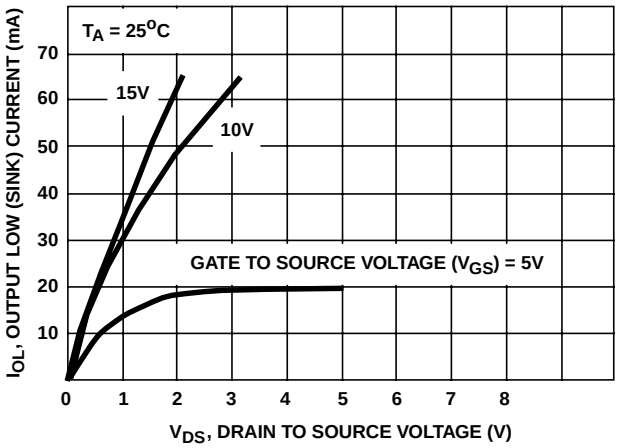


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

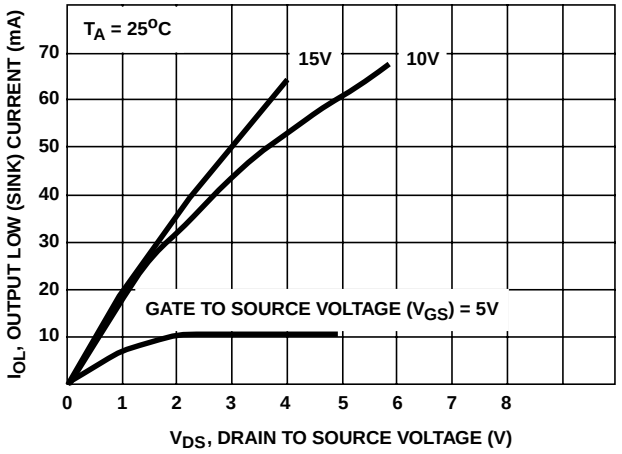


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

Typical Performance Curves (Continued)

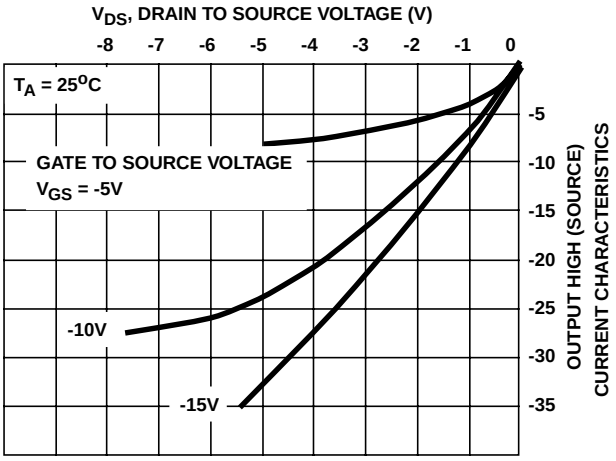


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

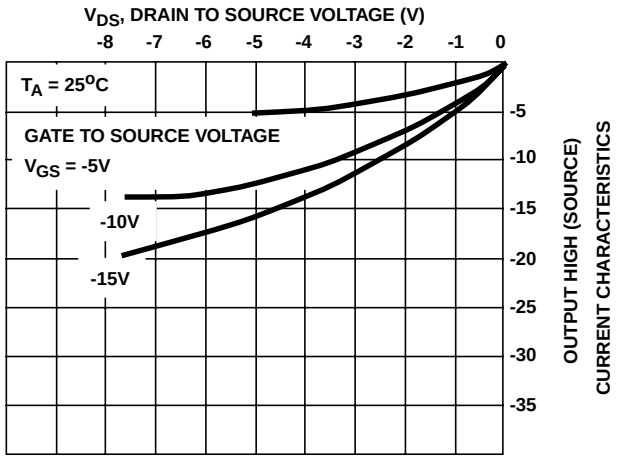


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

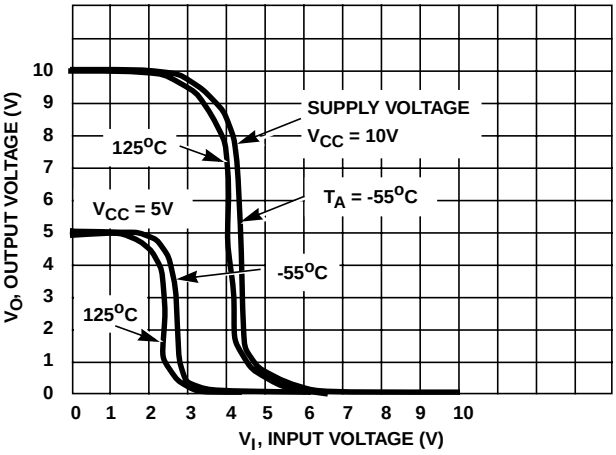


FIGURE 8. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4049UB

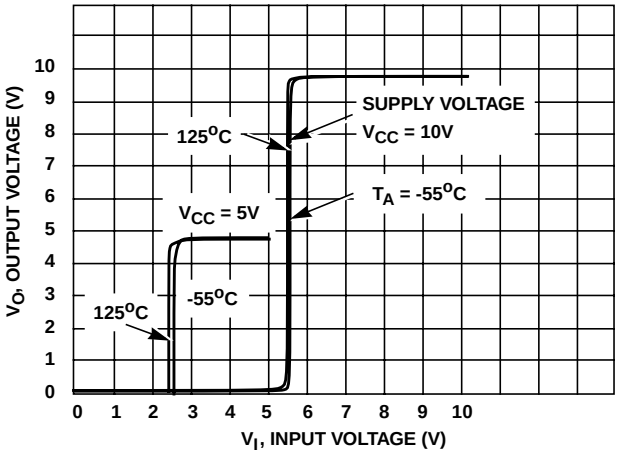


FIGURE 9. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4050B

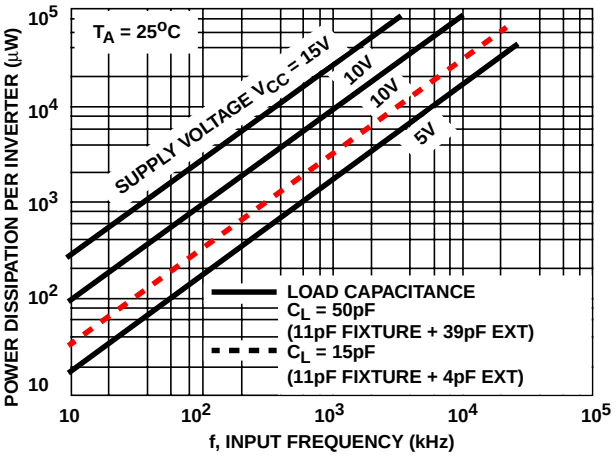


FIGURE 10. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

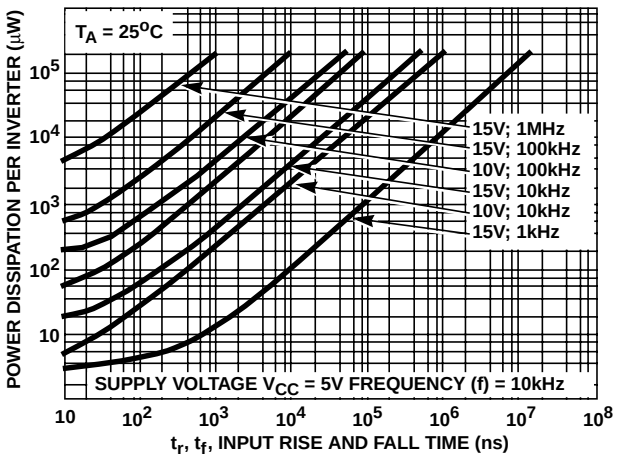


FIGURE 11. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4049UB

Typical Performance Curves (Continued)

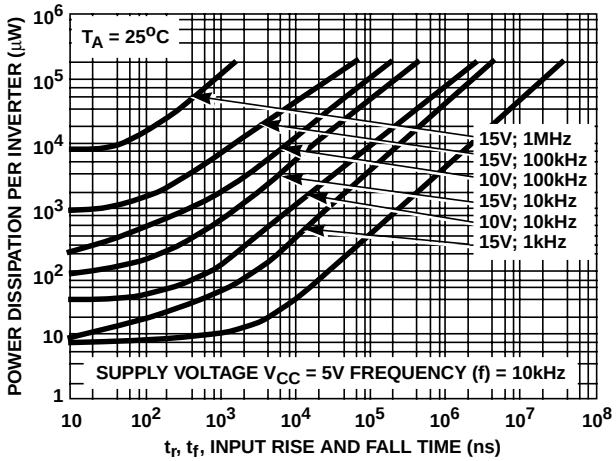


FIGURE 12. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4050B

Test Circuits

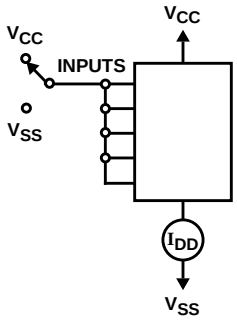
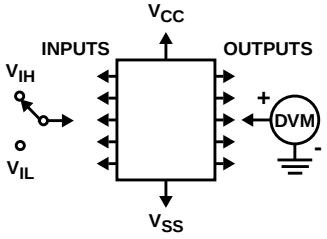
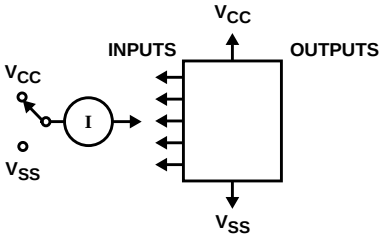


FIGURE 13. QUIESCENT DEVICE CURRENT TEST CIRCUIT



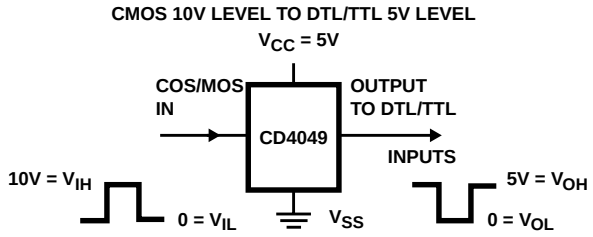
NOTE: Test any one input with other inputs at V_{CC} or V_{SS}.

FIGURE 14. INPUT VOLTAGE TEST CIRCUIT



NOTE: Measure inputs sequentially, to both V_{CC} and V_{SS} connect all unused inputs to either V_{CC} or V_{SS}.

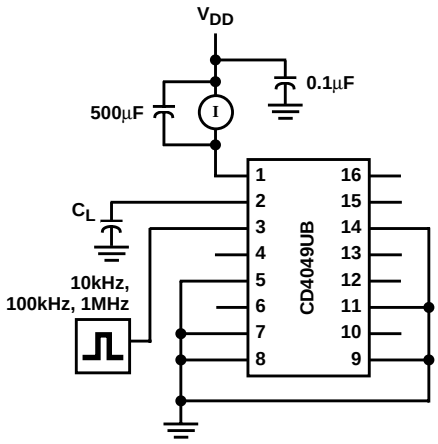
FIGURE 15. INPUT CURRENT TEST CIRCUIT



In Terminal - 3, 5, 7, 9, 11, or 14
Out Terminal - 2, 4, 6, 10, 12 or 15
V_{CC} Terminal - 1
V_{SS} Terminal - 8

FIGURE 16. LOGIC LEVEL CONVERSION APPLICATION

Test Circuits (Continued)



C_L INCLUDES FIXTURE CAPACITANCE

FIGURE 17. DYNAMIC POWER DISSIPATION TEST CIRCUITS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4049UBD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4049UBEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4049UBF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4049UBF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4049UBF3AS2283	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4049UBF3AS2534	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4049UBM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
CD4049UBM96	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
CD4049UBNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD4049UBPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4049UBPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDWE4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDWRE4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4050BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4050BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4050BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4050BF3AS2283	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4050BF3AS2534	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
CD4050BM	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
CD4050BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4050BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4050BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/05553BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
JM38510/05554BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type

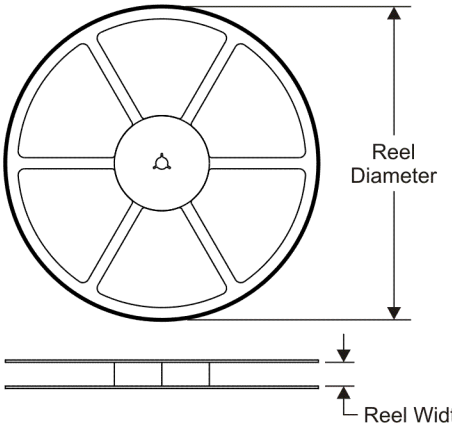
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

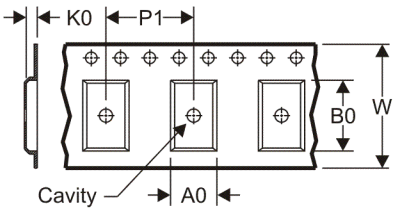
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

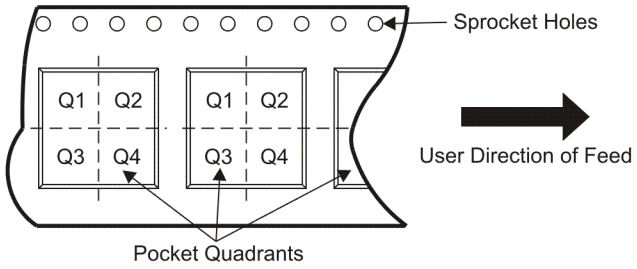


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

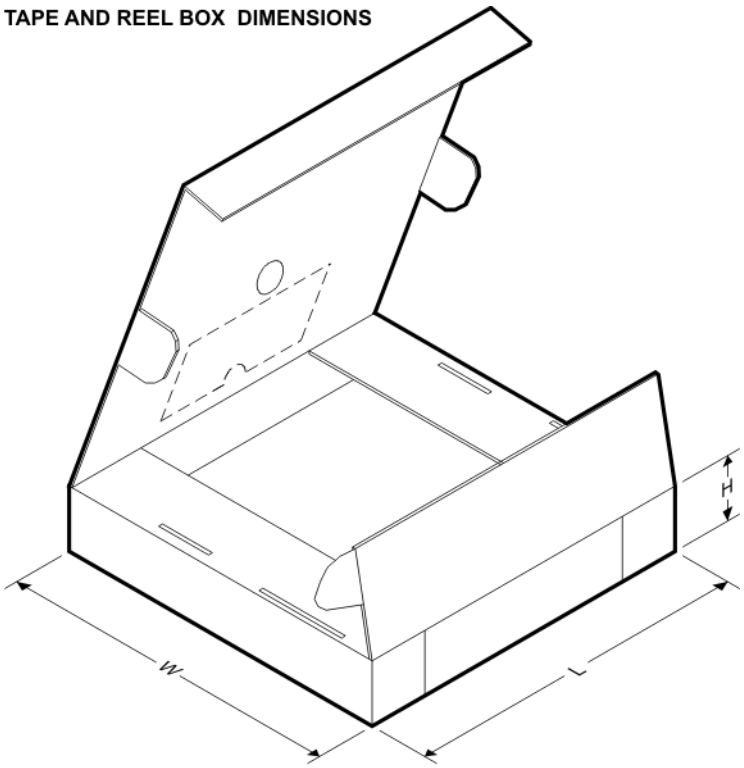
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4049UBDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4049UBDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD4049UBNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4049UBPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
CD4050BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4050BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
CD4050BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4050BPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



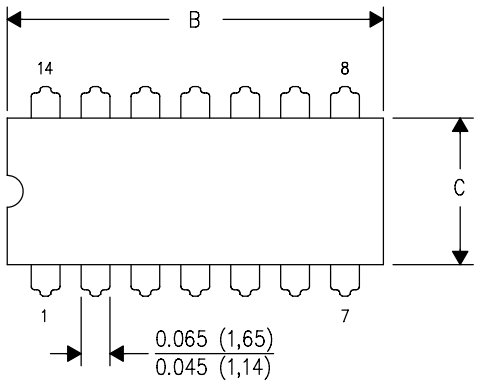
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4049UBDR	SOIC	D	16	2500	333.2	345.9	28.6
CD4049UBDWR	SOIC	DW	16	2000	346.0	346.0	33.0
CD4049UBNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4049UBPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
CD4050BDR	SOIC	D	16	2500	333.2	345.9	28.6
CD4050BDWR	SOIC	DW	16	2000	346.0	346.0	33.0
CD4050BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4050BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

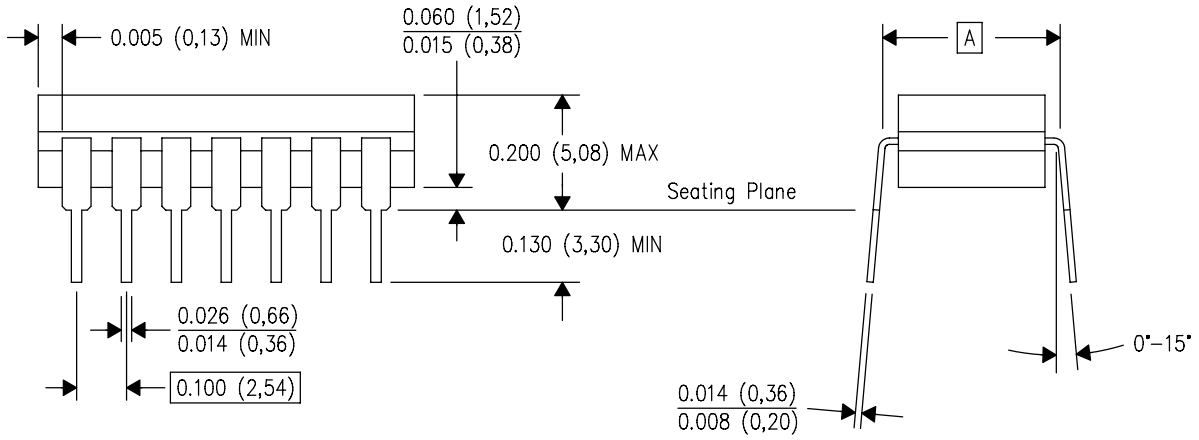
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



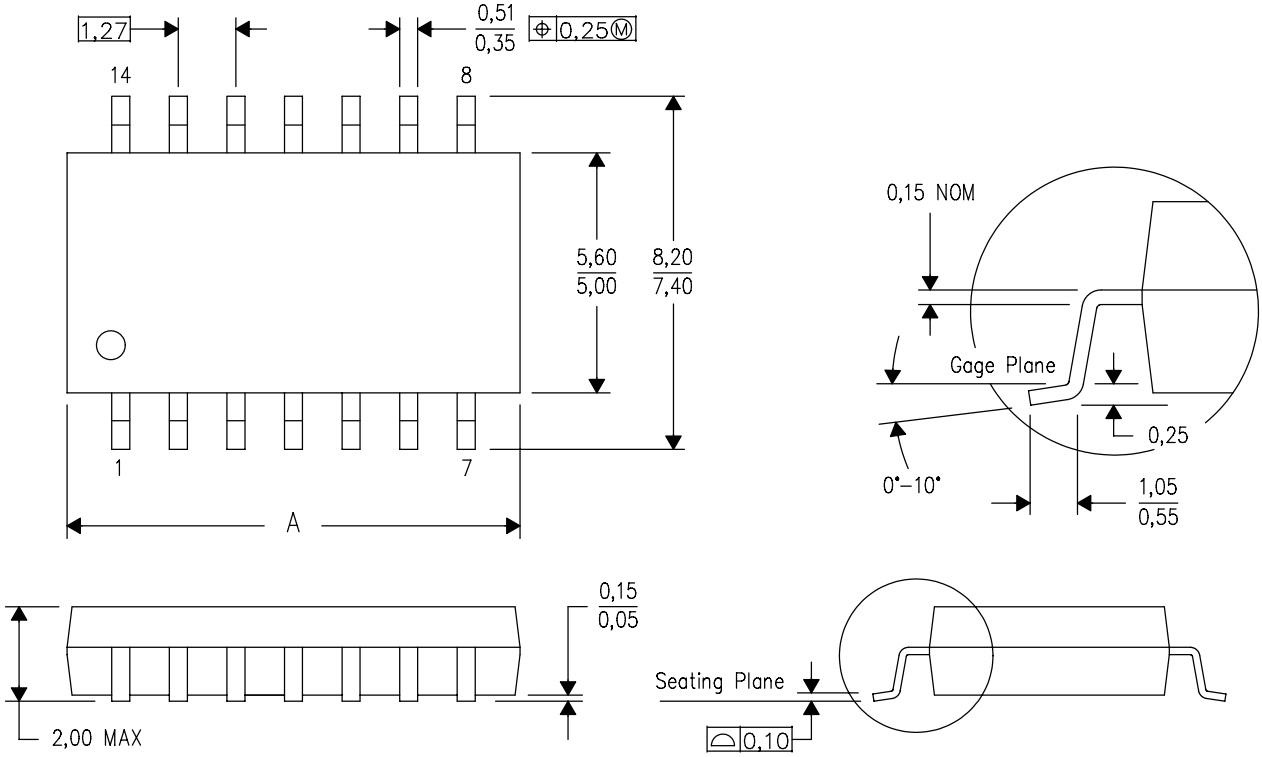
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



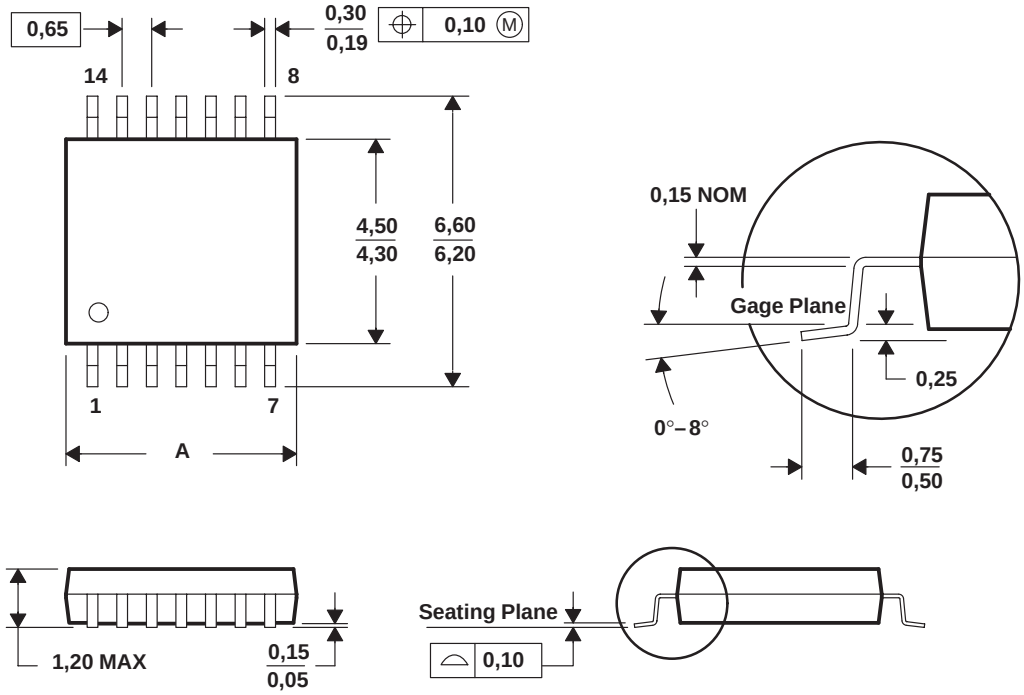
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

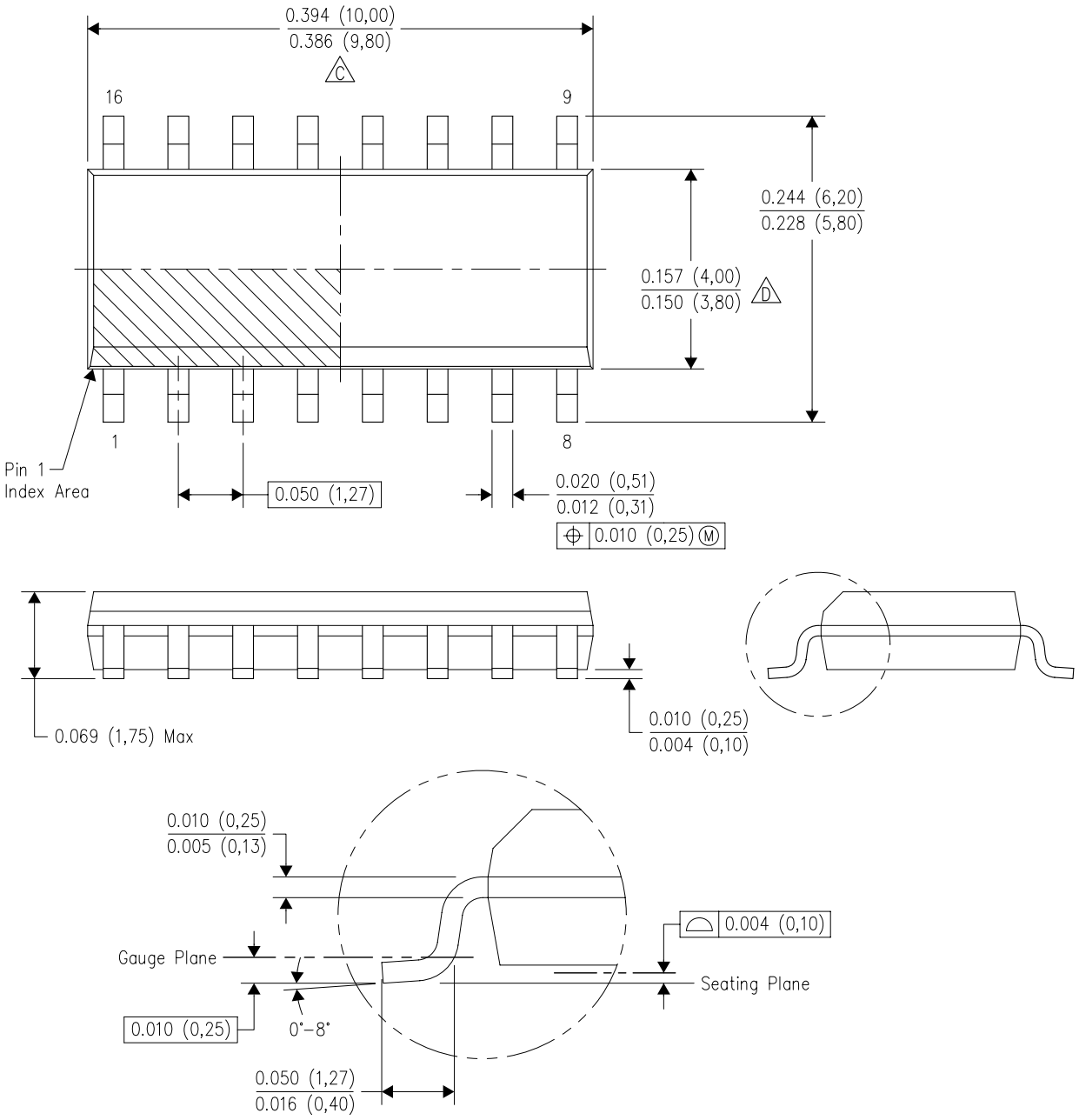


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

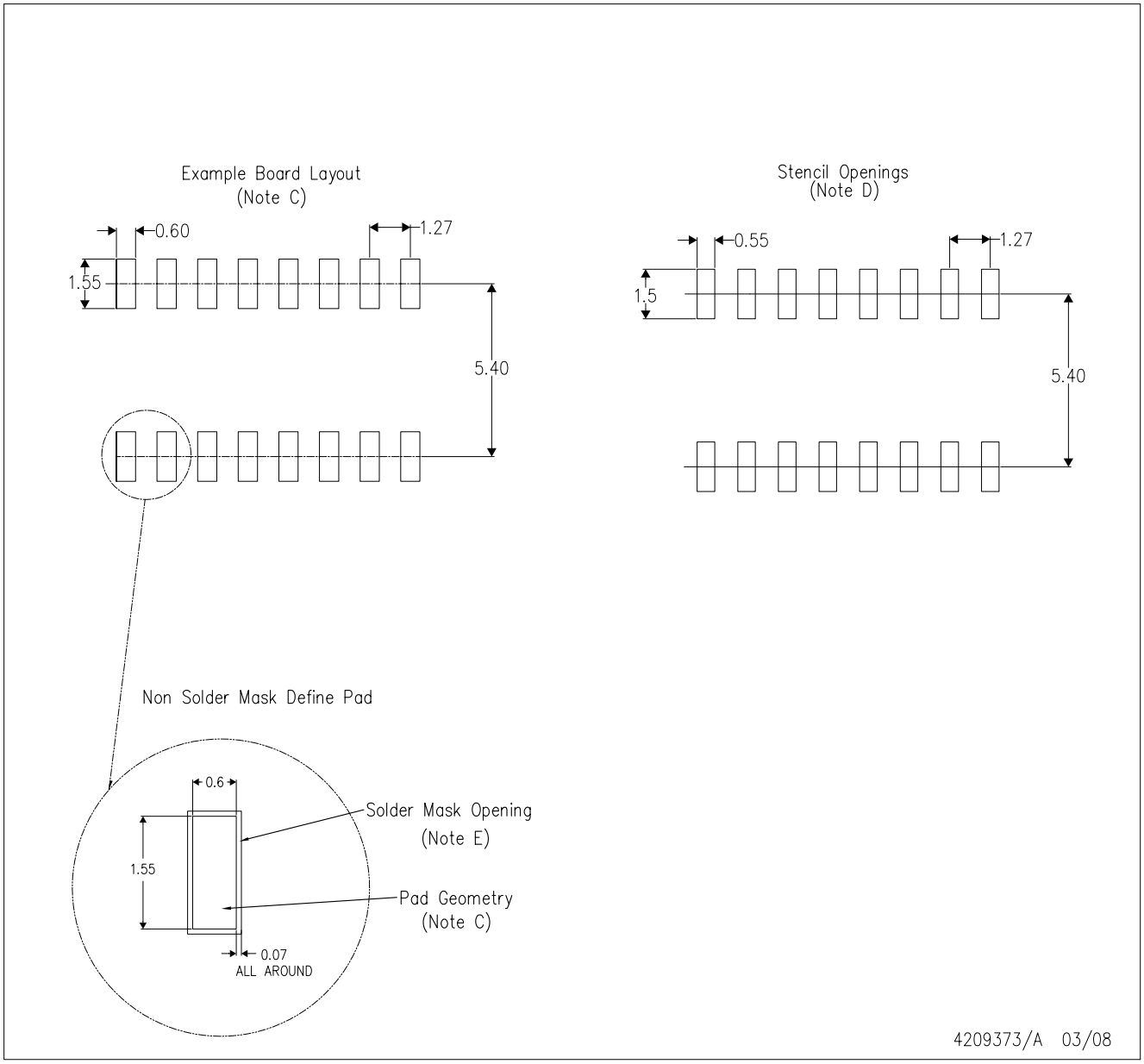
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



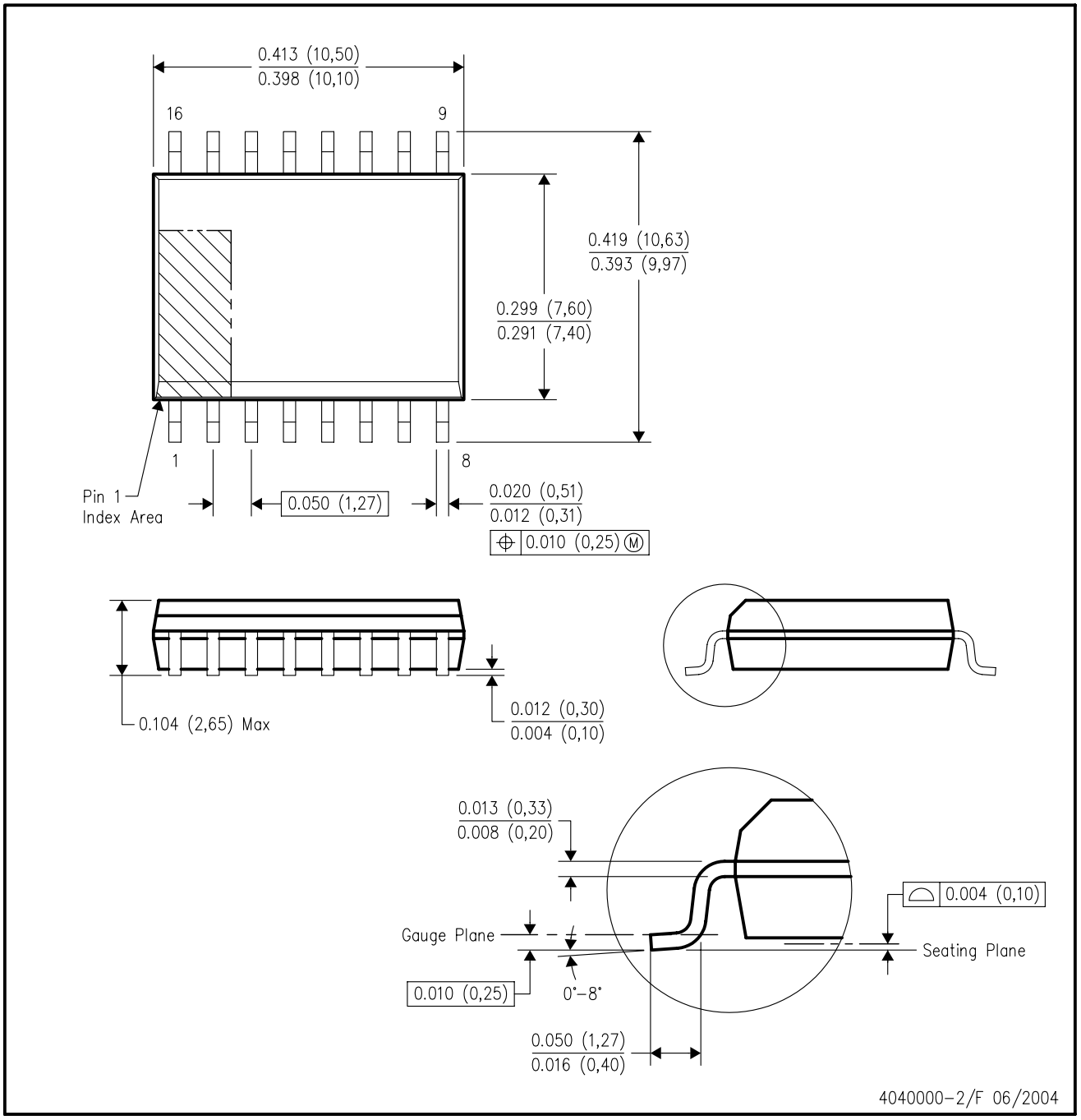
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

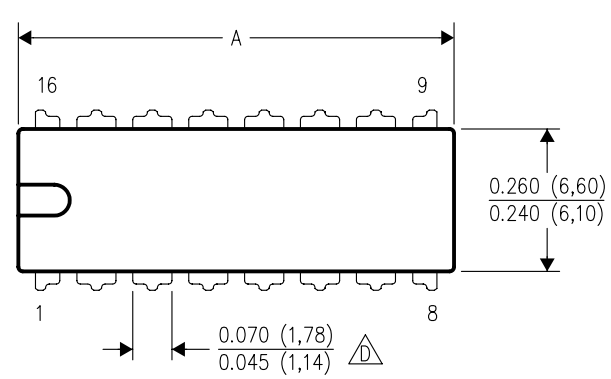


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

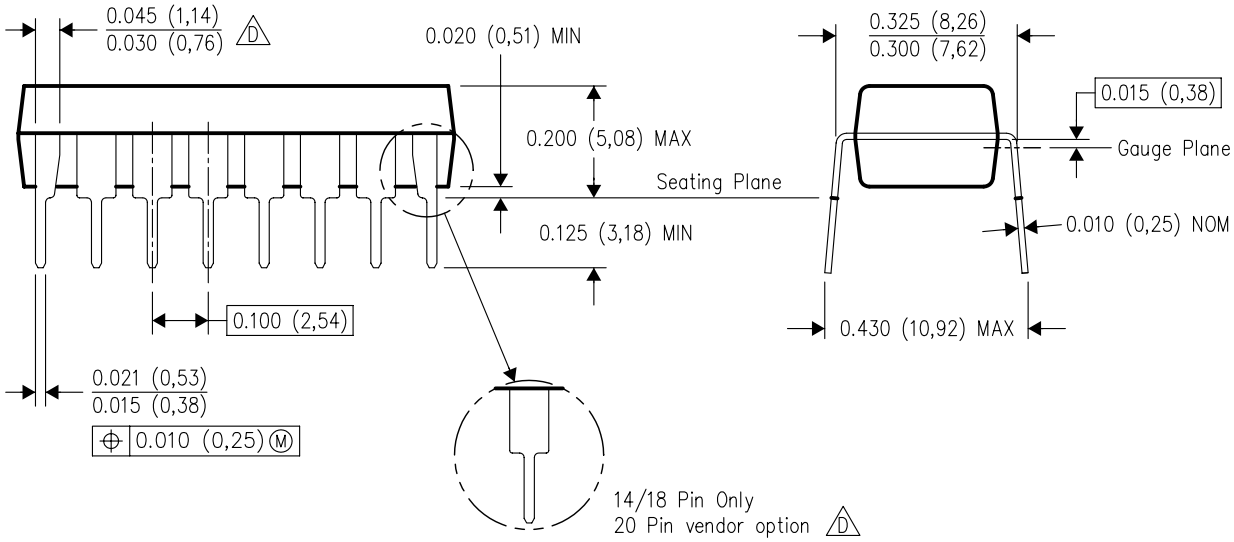
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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