

OptiMOS® Power-Transistor

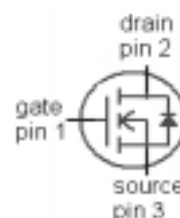
Features

- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (lead free)
- Ultra low Rds(on)
- 100% Avalanche tested

Product Summary

V_{DS}	55	V
$R_{DS(on),max}$ (SMD version)	14.4	mΩ
I_D	50	A

PG-TO252-3-11



Type	Package	Marking
IPD50N06S2-14	PG-TO252-3-11	PN0614

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	50 ¹⁾	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	49	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	200	
Avalanche energy, single pulse	E_{AS}	$I_D=50\text{ A}$	240	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	136	W
Operating and storage temperature	T_j , T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.1	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	100	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm ² cooling area ³⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=80\text{ }\mu\text{A}$	2.1	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=32\text{ A},$	-	10.8	14.4	m Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	1485	-	pF
Output capacitance	C_{oss}		-	464	-	
Reverse transfer capacitance	C_{rss}		-	167	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V},$ $I_D=50\text{ A}, R_G=7.5\ \Omega$	-	13	-	ns
Rise time	t_r		-	29	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Fall time	t_f		-	19	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=44\text{ V}, I_D=50\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	8	11	nC
Gate to drain charge	Q_{gd}		-	16	24	
Gate charge total	Q_g		-	39	52	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	-	-	50	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=50\text{ A},$ $T_j=25\text{ °C}$	-	1	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	45	-	ns
Reverse recovery charge ²⁾	Q_{rr}	$V_R=30\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	74	-	nC

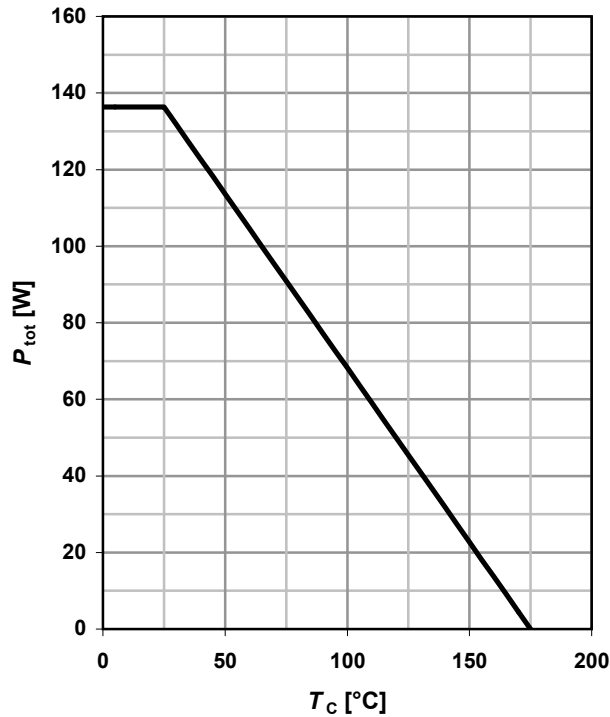
¹⁾ Current is limited by bondwire; with an $R_{thJC}=1.1\text{ K/W}$ the chip is able to carry 69 A. For detailed information see Application Note ANPS071E at www.infineon.com/optimos

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

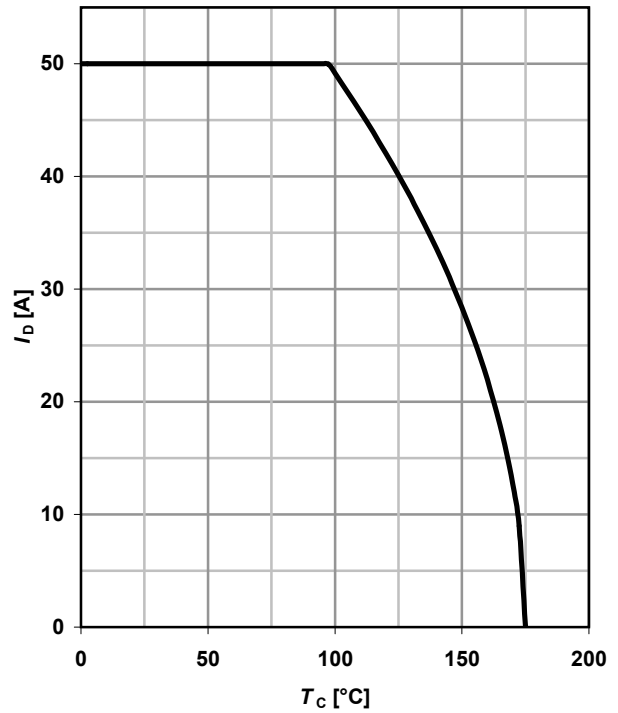
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

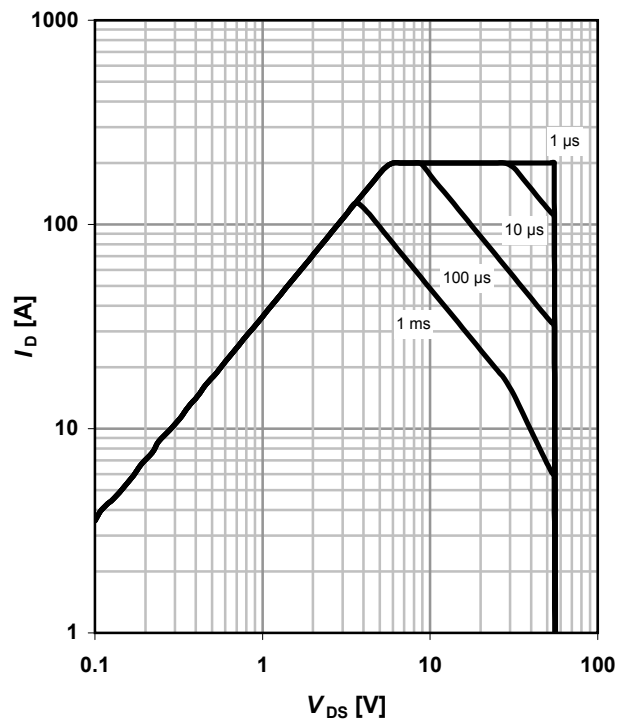
$$I_D = f(T_C); V_{\text{GS}} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

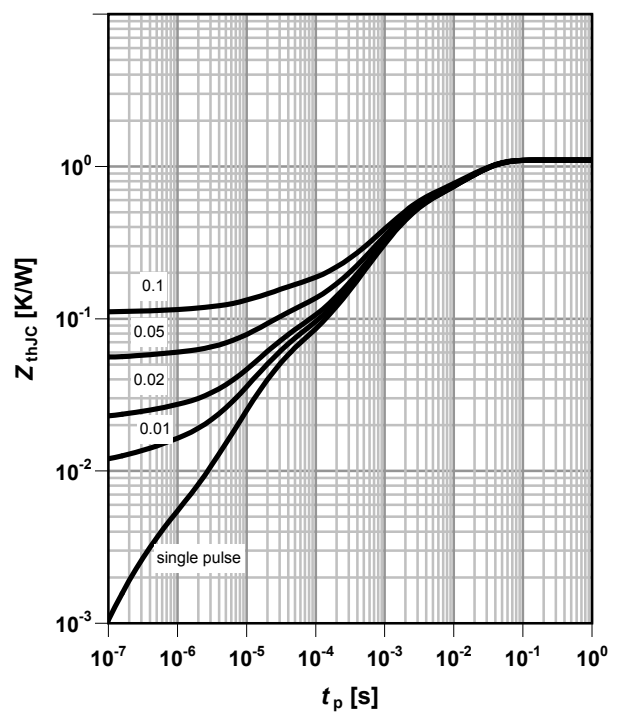
parameter: t_p



4 Max. transient thermal impedance

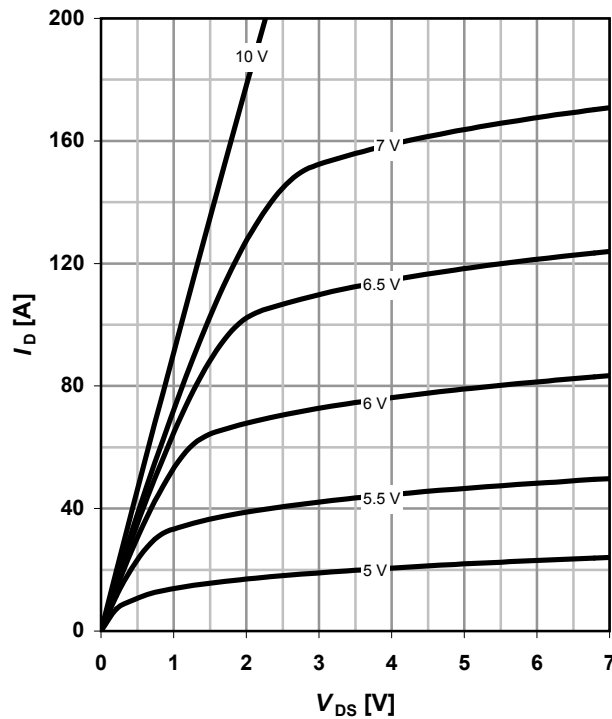
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



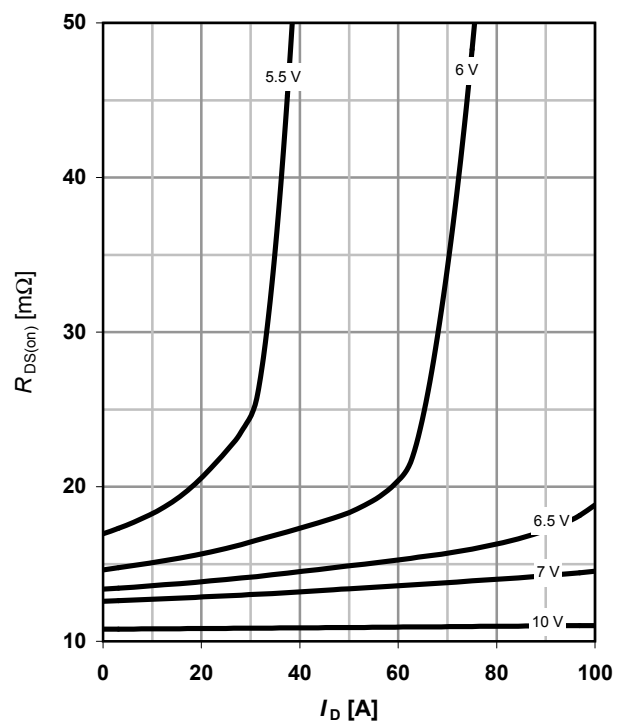
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


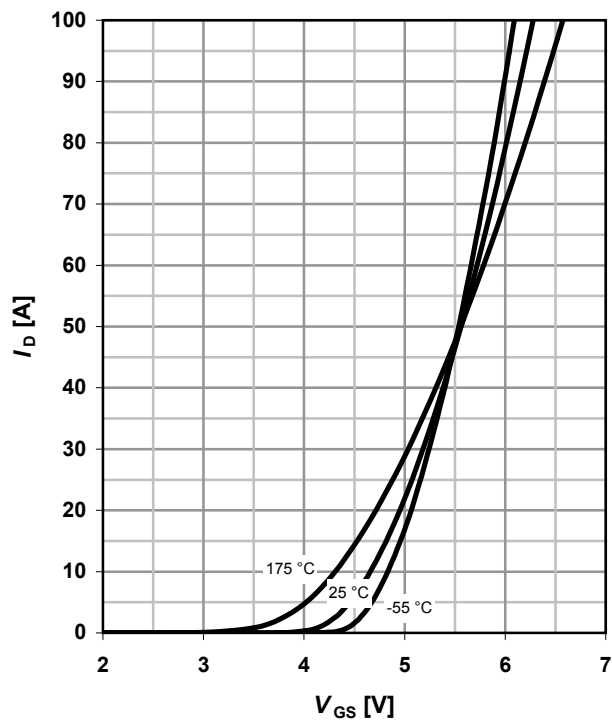
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


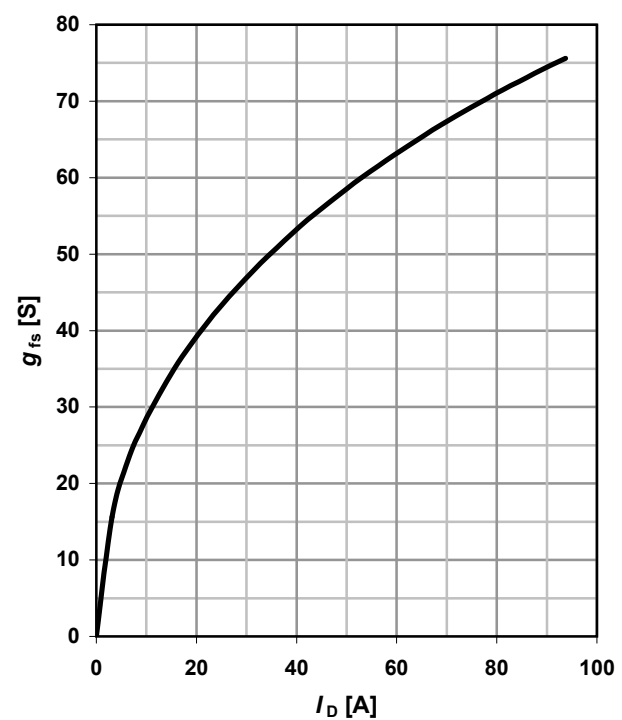
7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{V}$

parameter: T_j


8 Typ. Forward transconductance

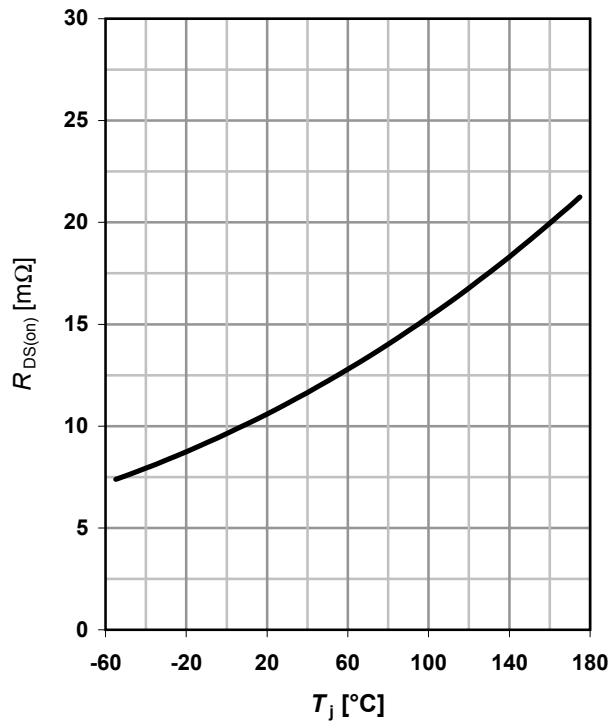
 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

parameter: g_{fs}


9 Typ. Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

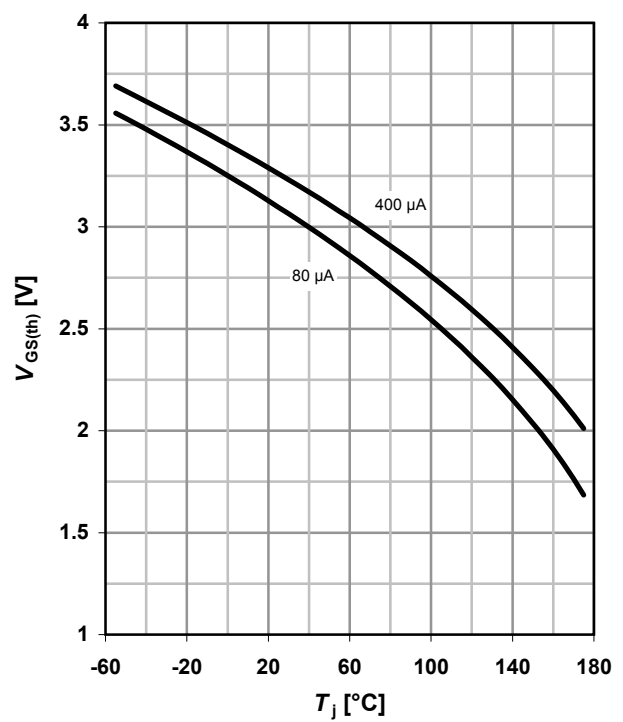
parameter: $I_D = 32 \text{ A}$; $V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

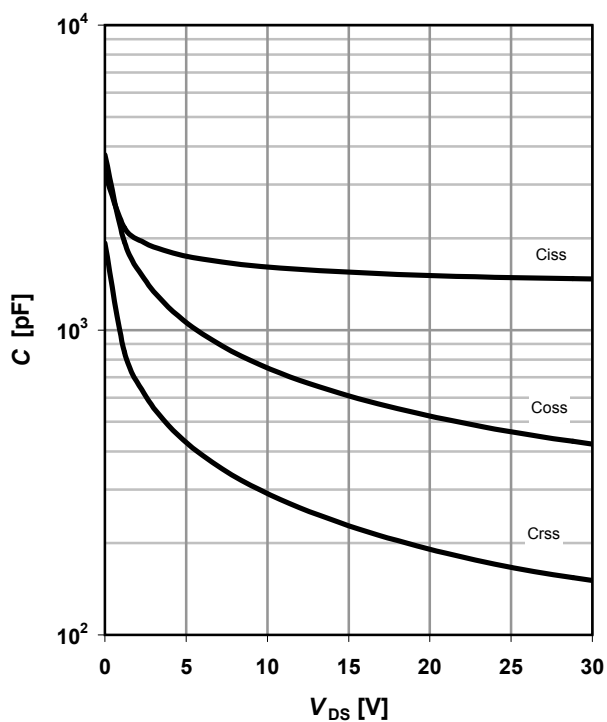
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. capacitances

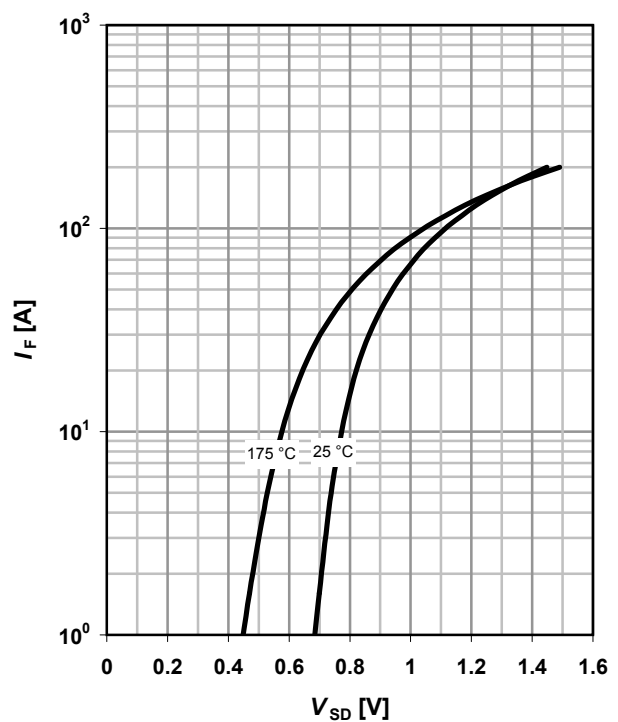
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

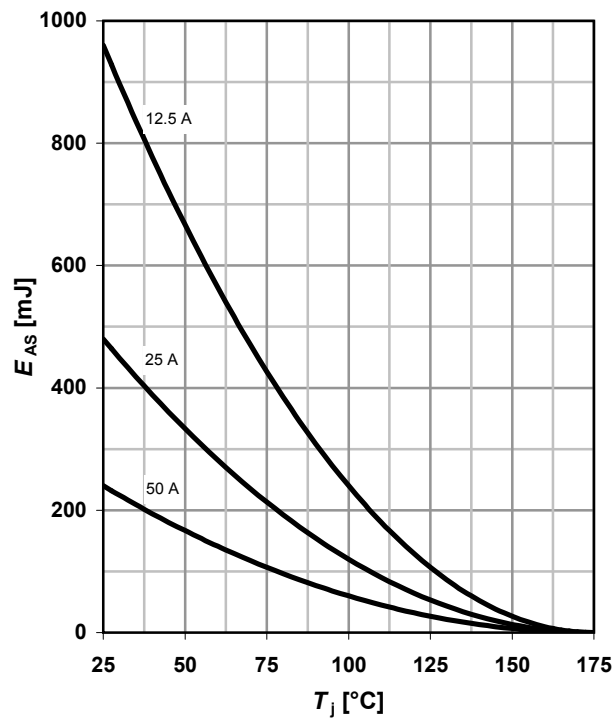
parameter: T_j



13 Typical avalanche energy

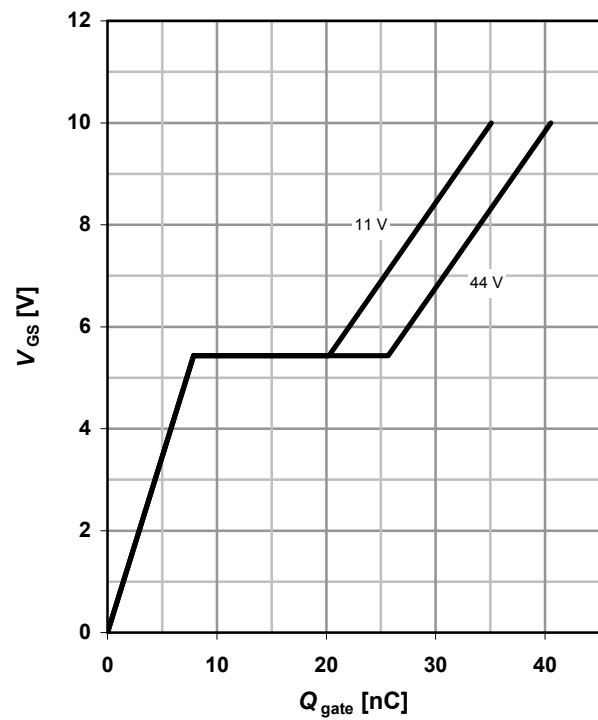
$$E_{AS} = f(T_j)$$

parameter: I_D



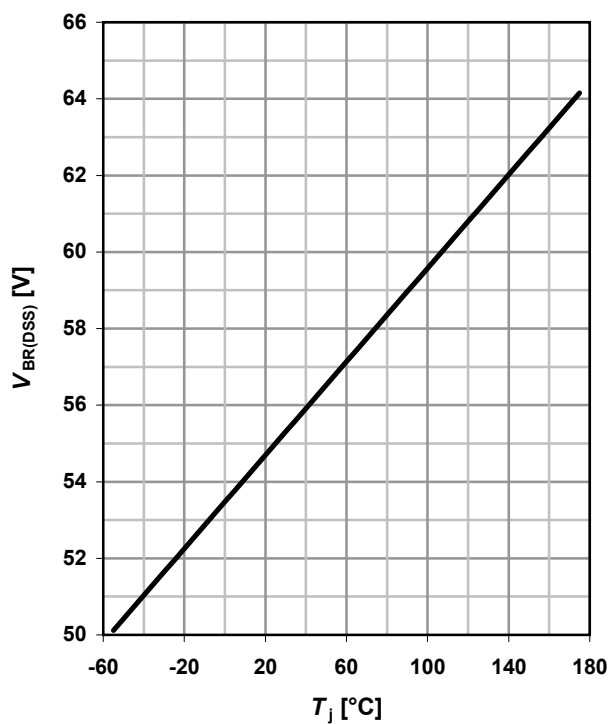
14 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 50 \text{ A pulsed}$$

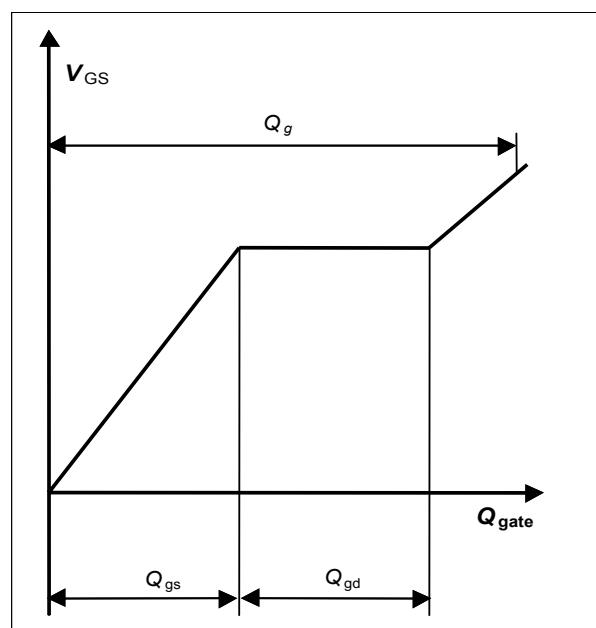


15 Typ. drain-source breakdown voltage

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



16 Gate charge waveforms



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Infineon Technologies AG
81726 Munich, Germany

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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.1	20.10.2008	Correction of RthJC from 3.4K/W to 1.1K/W