2SK4047-01S

Automotive

FUJI POWER MOSFET

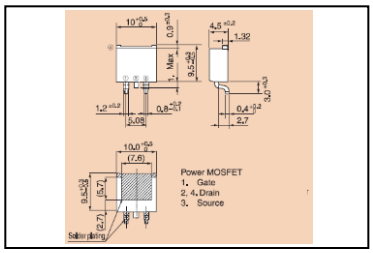
Trench Power MOSFET (2nd Gen.) series

N-Channel enhancement mode power MOSFET

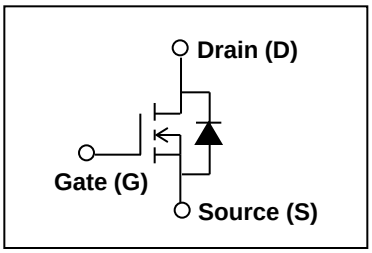
■Features

Low on-state resistance
Low switching loss
100% avalanche tested

■Outline Drawings [mm]



■Equivalent circuit schematic



■Applications

Automotive switching applications

■Absolute Maximum Ratings at Tc=25℃(unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	60	V	
	V_{DSX}	30	V	V_{GS}=-20V
Continuous Drain Current	I_D	±80	A	
Pulsed Drain Current	I_{DP}	±320	A	
Gate-Source Voltage	V_{GS}	+30/-20	V	
Non-Repetitive Maximum Avalanche current	I_{AS}	80	A	Note*1
Non-Repetitive Maximum Avalanche Energy	E_{AS}	274.5	mJ	Note*2
Maximum Power Dissipation	P_D	195	W	
Operating and Storage Temperature range	T_{ch}	150	℃	
	T_{stg}	-55 to +150	℃	

Note*1 : Tch≦150℃,See Fig.1 and Fig.2
Note*2 : Starting Tch=25℃,L=28.6μH,V_{CC}=48V,RG=50Ω,See Fig.1 and Fig.2
E_{AS} limited by maximum channel temperature and avalanche current.
See to Avalanche Energy graph of page 4

■Electrical Characteristics at Tc=25℃(unless otherwise specified)

Static Ratings

Description	Symbol	Conditions		Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1mA V_{GS}=0V		60	—	—	V
	BV_{DSX}	I_D=1mA V_{GS}=-20V		30	—	—	V
Gate Threshold Voltage	$V_{GS(th)}$	I_D=10mA V_{DS}= V_{GS}		2.5	3.0	3.5	V
Zero Gate Voltage Drain current	I_{DSS}	V_{DS}= 60V V_{GS}=0V	Ta=25℃	—	1	100	μA
Gate-Source Leakage current	I_{GSS}	V_{GS}=+30V/-20V V_{DS}= 0V		—	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	I_D=40A V_{GS}=10V		—	5.0	6.5	mΩ

Dynamic Ratings

Description	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Transconductance	g_{fS}	I_D=40A V_{DS}=10V	25	45	—	S
Input Capacitance	C_{iSS}	V_{DS}=25V V_{GS}=0V f=1MHz	—	4500	—	pF
Output Capacitance	C_{oSS}		—	950	—	
Reverse Transfer Capacitance	C_{rSS}		—	450	—	
Turn-On Time	$t_{d(on)}$	V_{CC}=30V, V_{GS}=10V I_D=80A, R_G=10Ω See Fig.3 and Fig.4	—	35	—	ns
	t_r		—	45	—	
Turn-Off Time	$t_{d(off)}$		—	80	—	
	t_f		—	55	—	
Total Gate Charge	Q_G	V_{DD}=30V, I_D=80A V_{GS}=10V See Fig.5	—	95	—	nC
Gate-Source Charge	Q_{GS}		—	30	—	
Gate-Drain Charge	Q_{GD}		—	20	—	

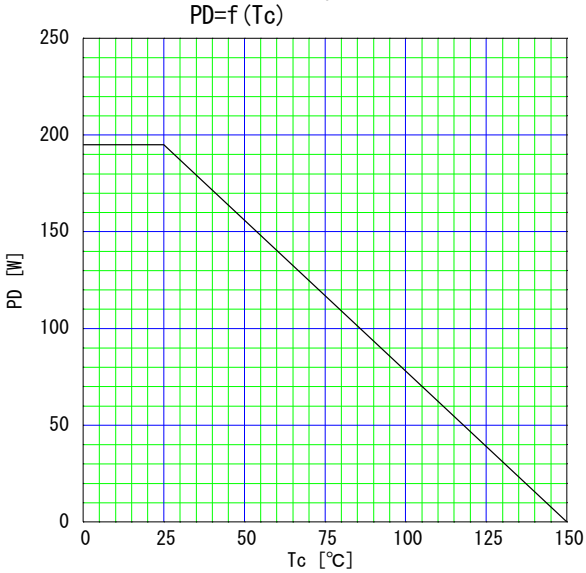
Reverse Ratings

Description	Symbol	Conditions	Min.	Typ.	Max.	Unit
Avalanche Capability	I_{AV}	L=28.6μH, T_{ch}=25℃ See Fig.1 and Fig.2	80	—	—	A
Diode Forward On- Voltage	V_{SD}	I_F=80A, V_{GS}=0V T_{ch}=25℃	—	0.95	1.5	V
Reverse Recovery Time	t_{rr}	I_F=40A, V_{GS}=0V -di/dt=100A/μs T_{ch}=25℃	—	150	—	ns
Reverse Recovery Charge	Q_{rr}		—	0.18	—	μC

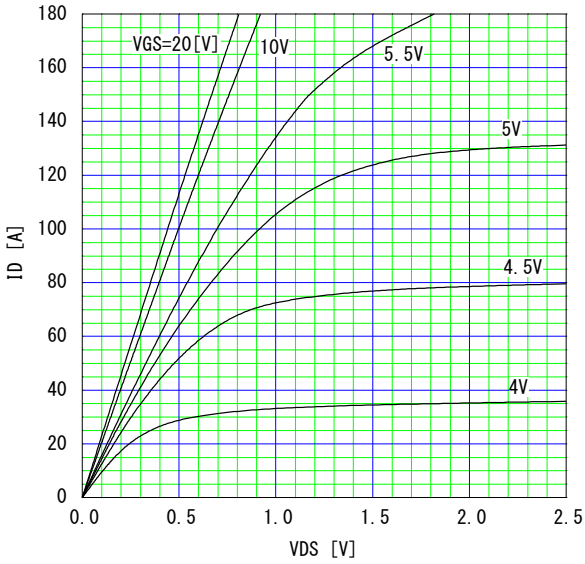
■Thermal Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Cannel to Case	$R_{th(ch-c)}$	—	—	0.641	℃/W
Cannel to Ambient	$R_{th(ch-a)}$	—	—	75.0	℃/W

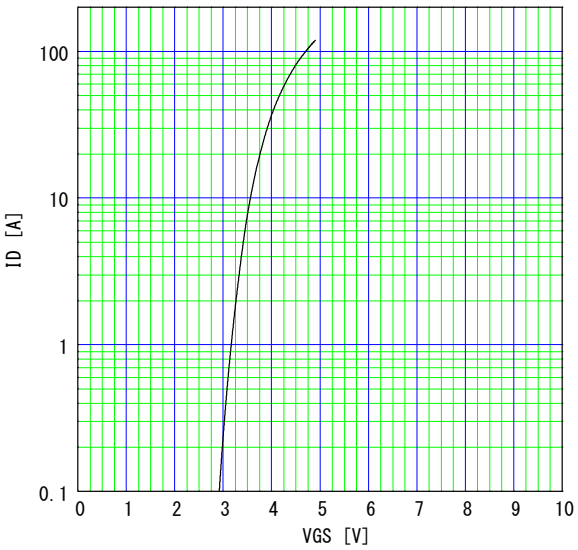
Power Dissipation
PD=f(Tc)



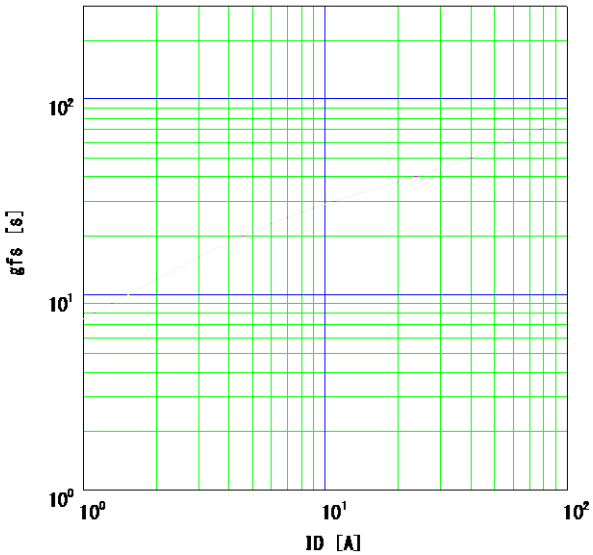
Typical output characteristics
ID=f(VDS):80μs pulse test, Tc=25℃



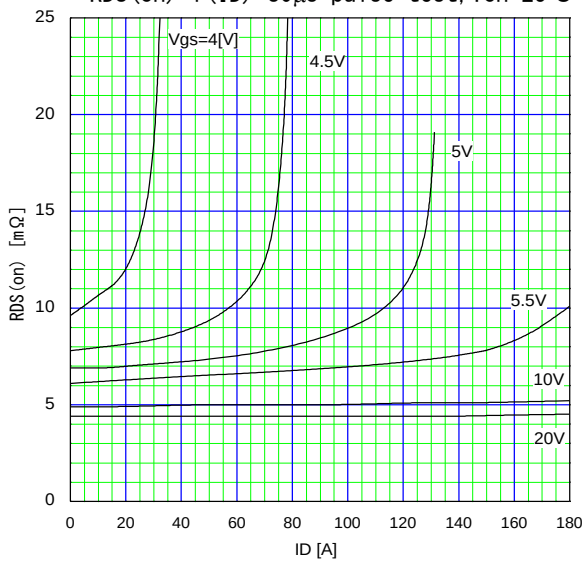
Typical transfer characteristics
ID=f(VGS):80μs pulse test, VDS=10V, Tch=25℃



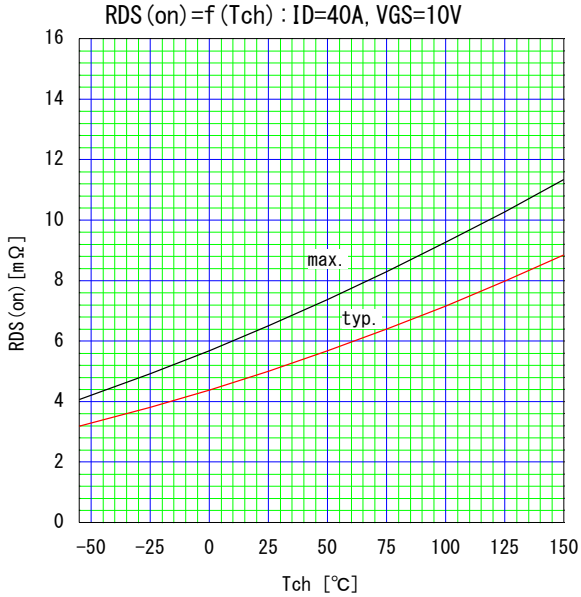
Typical forward transconductance
gfs=f(ID):80μs pulse test, VDS=10V, Tch=25℃



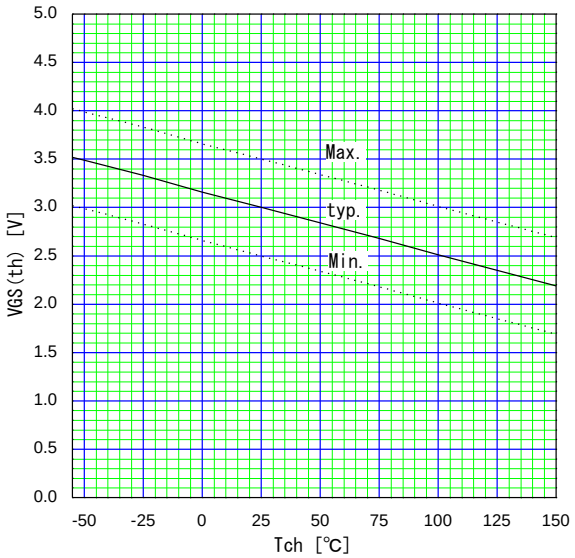
Typical Drain-Source on-State Resistance
RDS(on)=f(ID):80μs pulse test, Tch=25℃



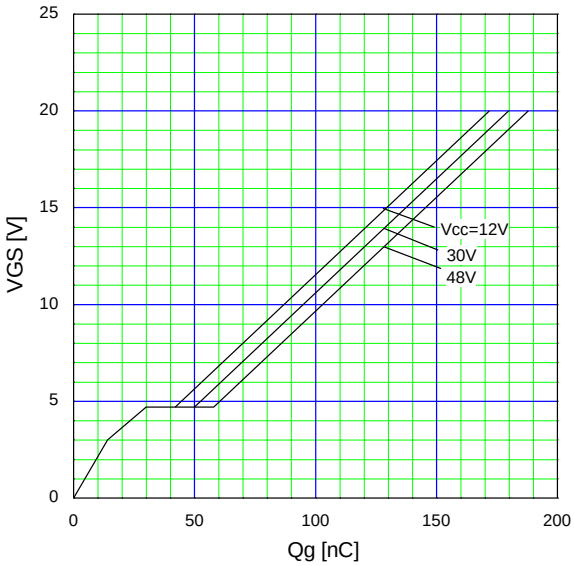
Drain-source on-state resistance
RDS(on)=f(Tch):ID=40A, VGS=10V



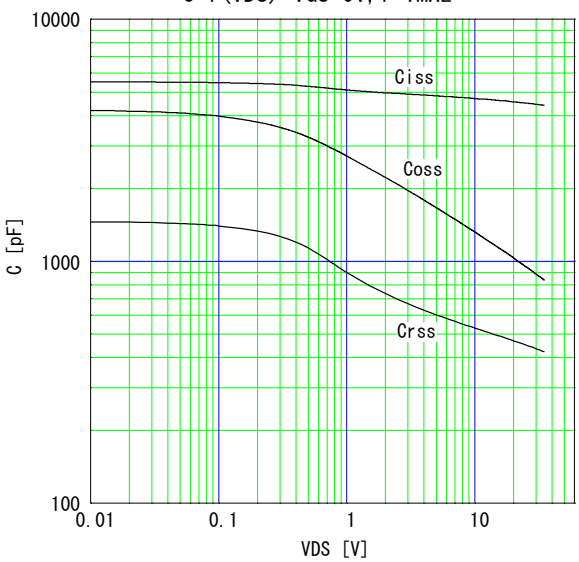
Gate Threshold Voltage vs. Tch
VGS(th)=f(Tch):VDS=VGS, ID=10mA



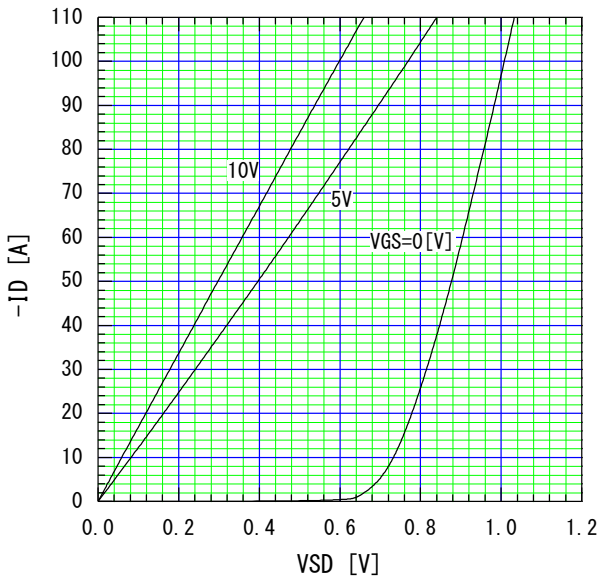
Typical Gate Charge Characteristics
VGS=f(Qg):ID=80A, Tch=25℃



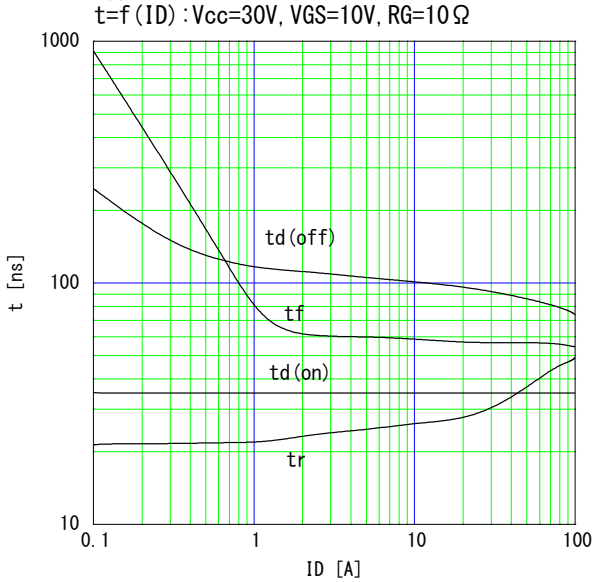
Typical capacitances
C=f(VDS):VGS=0V, f=1MHz



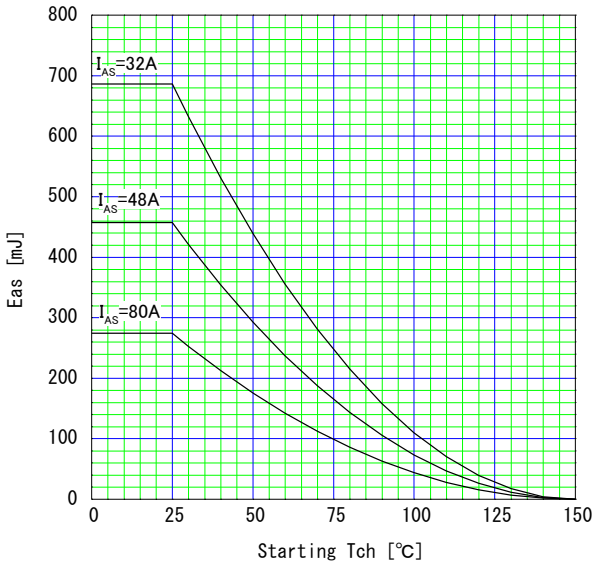
Typical Forward Characteristics of Reverse Diode
-ID=f(VSD):80μs pulse test, Tch=25℃



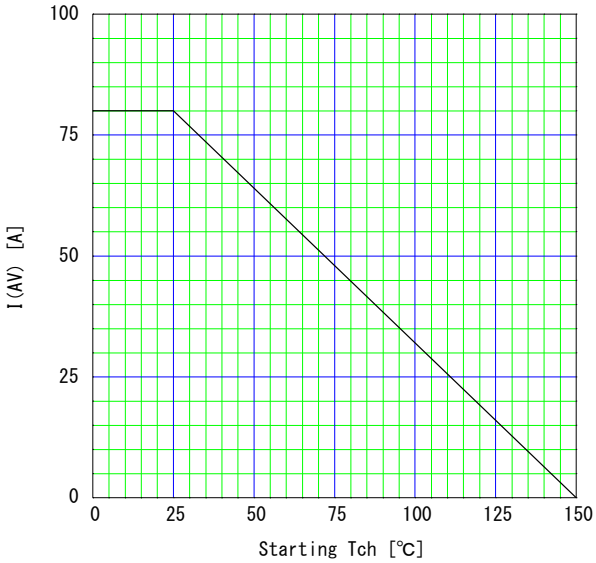
Typical Switching Characteristics vs. ID
t=f(ID):Vcc=30V, VGS=10V, RG=10Ω



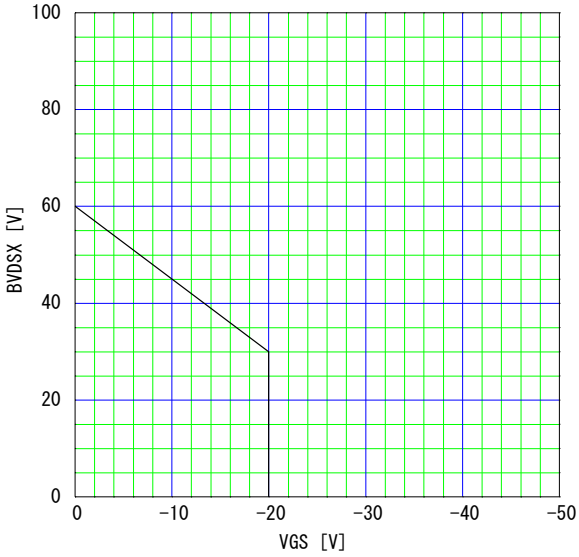
Maximum Avalanche energy vs. starting Tch
Eas=f(starting Tch):Vcc=48V, I_{AV}≦80A , single pulse



Maximum Avalanche Current vs. starting Tch
I(AV)=f(starting Tch) , single pulse



Drain-Sourse Breakdown Voltage vs. Vgs
BVDSX=f(VGS):Tch=25℃



Maximum Transient Thermal Impedance
Zth(ch-c)=f(t):D=0

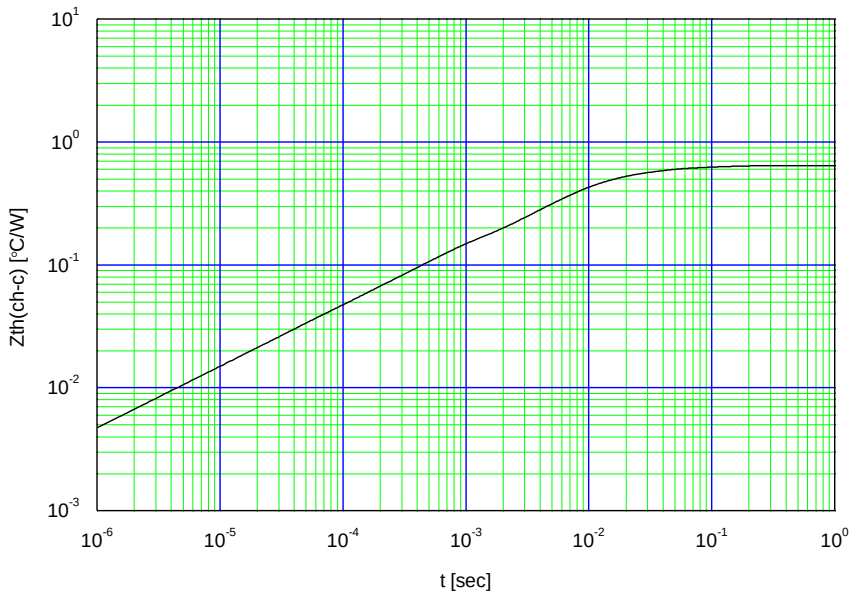


Fig.1 Avalanche Test circuit

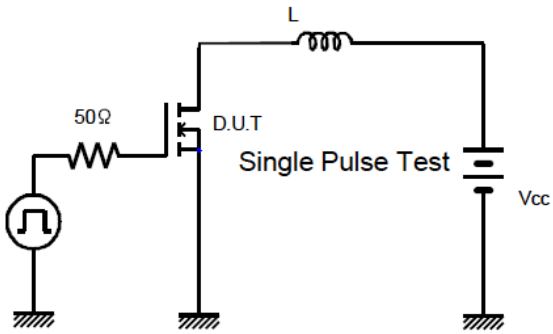


Fig.2 Operating waveforms of Avalanche Test

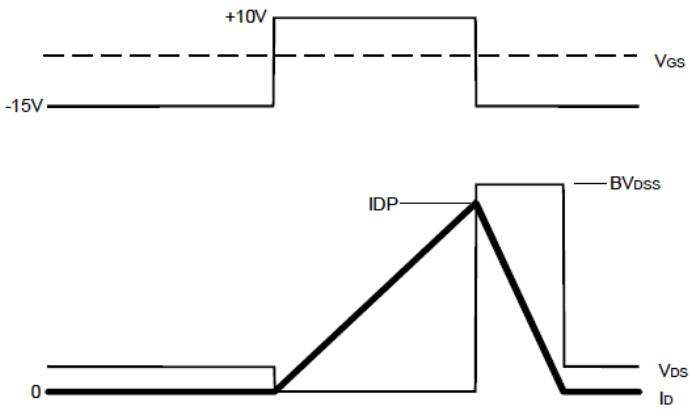


Fig.3 Switching Test circuit

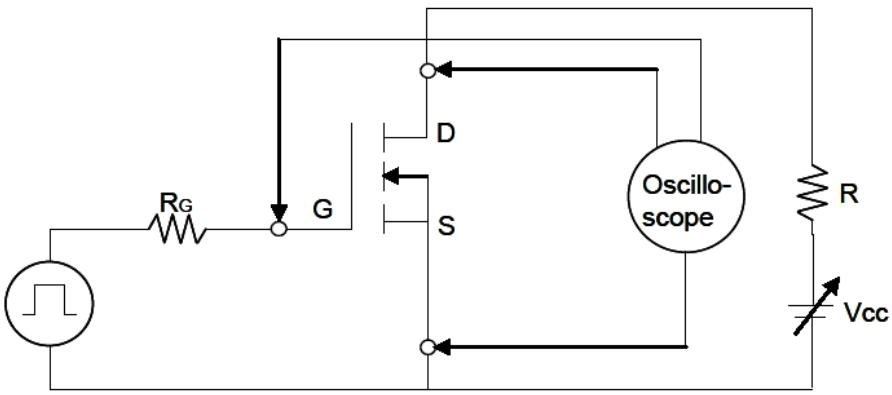


Fig.4 Operating waveform of Switching Test

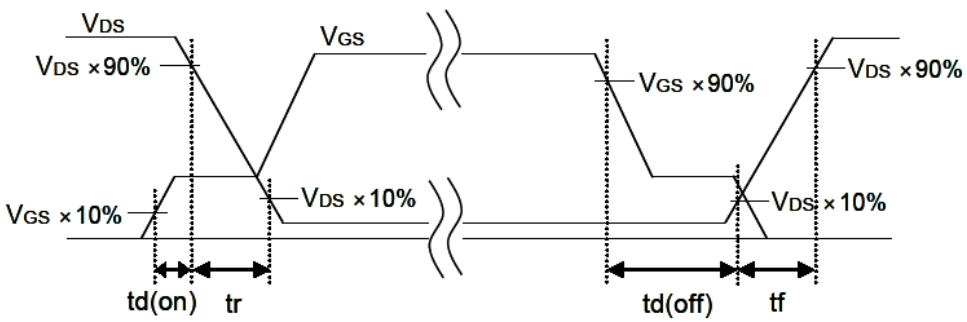


Fig.5 Operating waveform of Gate charge Test

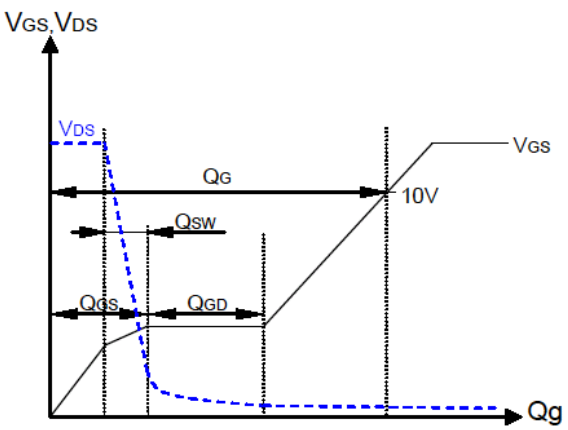
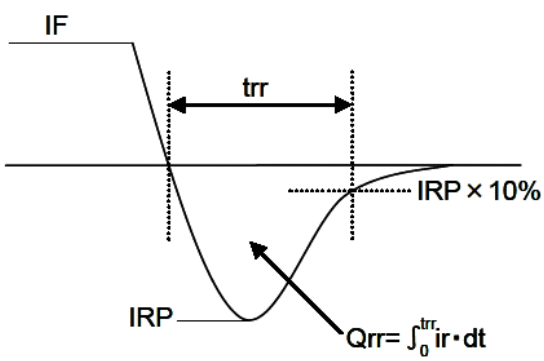


Fig.6 Operating waveform of Body diode Recovery Test



■Out view

FUJI POWER MOS FET

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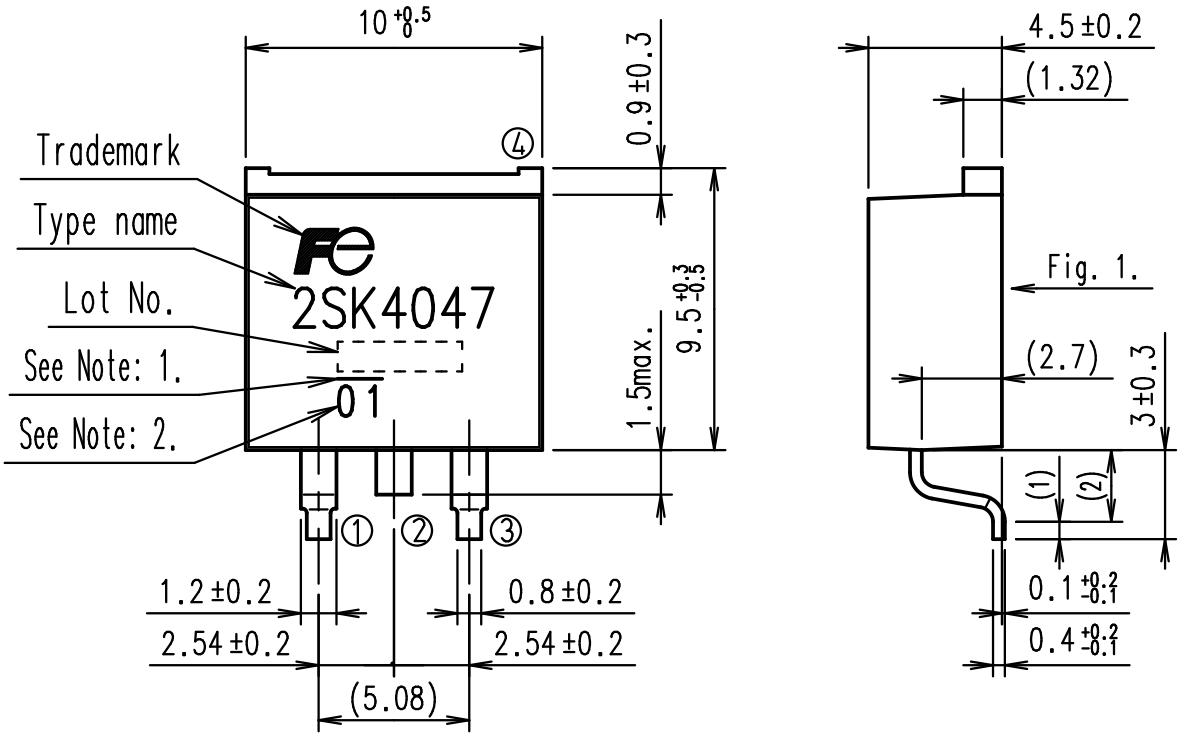
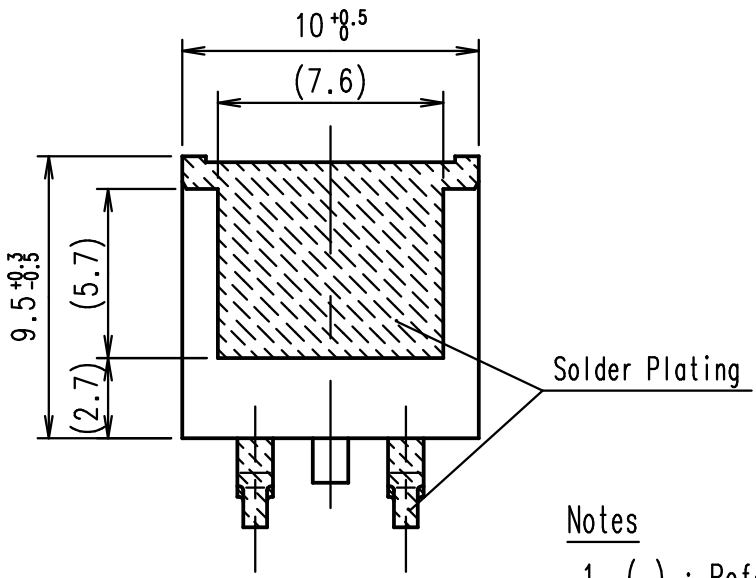


Fig. 1.



CONNECTION

① GATE
④ ② DRAIN
③ SOURCE

Notes

1. ( ) : Reference dimensions.
2. The metal part is covered with the solder plating, part of cutting is without the solder plating.

DIMENSIONS ARE IN MILLIMETERS.

Note: 1. Mark of the Lead-Free Solder.
(Solder plating which covers the metal)
2. Guaranteed mark of
avalanche ruggedness.

WARNING

1.This Data Sheet contains the product specifications, characteristics, data, materials, and structures as of Jul 2013.

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・Nuclear control equipment ・Submarine repeater equipment

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