

FMP10N60S1

FUJI POWER MOSFET

Super J-MOS series

N-Channel enhancement mode power MOSFET

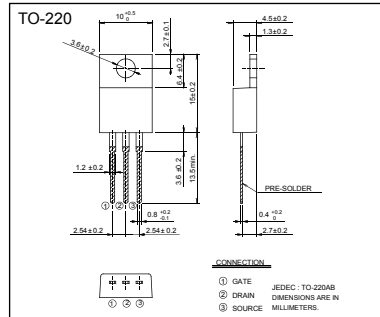
■ Features

- Low on-state resistance
- Low switching loss
- easy to use (more controllable switching dV/dt by R_g)

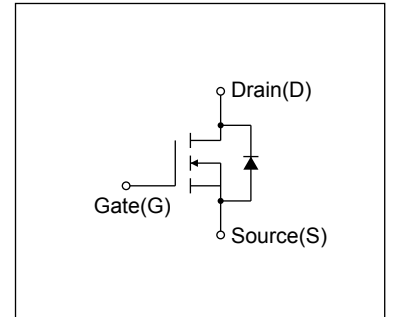
■ Applications

- UPS
- Server
- Telecom
- Power conditioner system
- Power supply

■ Outline Drawings [mm]



■ Equivalent circuit schematic



■ Absolute Maximum Ratings at $T_c=25^\circ\text{C}$ (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V_{DS}	600	V	
	V_{DSX}	600	V	$V_{GS}=-30\text{V}$
Continuous Drain Current	I_D	± 10	A	$T_c=25^\circ\text{C}$ Note*1
		± 6.3	A	$T_c=100^\circ\text{C}$ Note*1
Pulsed Drain Current	I_{DP}	± 30	A	
Gate-Source Voltage	V_{GS}	± 30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I_{AR}	2.9	A	Note *2
Non-Repetitive Maximum Avalanche Energy	E_{AS}	320	mJ	Note *3
Maximum Drain-Source dV/dt	d V_{DS} /dt	50	kV/ μs	$V_{DS}\leq 600\text{V}$
Peak Diode Recovery dV/dt	dV/dt	15	kV/ μs	Note *4
Peak Diode Recovery -di/dt	-di/dt	100	A/ μs	Note *5
Maximum Power Dissipation	P_D	2.02	W	$T_a=25^\circ\text{C}$
		90		$T_c=25^\circ\text{C}$
Operating and Storage Temperature range	T_{ch}	150	$^\circ\text{C}$	
	T_{stg}	-55 to +150	$^\circ\text{C}$	

Note *1 : Limited by maximum channel temperature.

Note *2 : $T_{ch}\leq 150^\circ\text{C}$, See Fig.1 and Fig.2

Note *3 : Starting $T_{ch}=25^\circ\text{C}$, $I_{AS}=1.8\text{A}$, $L=181\text{mH}$, $V_{DD}=60\text{V}$, $R_G=50\Omega$, See Fig.1 and Fig.2
 E_{AS} limited by maximum channel temperature and avalanche current.

Note *4 : $I_F\leq I_D$, -di/dt=100A/ μs , $V_{DD}\leq 400\text{V}$, $V_{peak}\leq BV_{DSS}$, $T_{ch}\leq 150^\circ\text{C}$.

Note *5 : $I_F\leq I_D$, dV/dt=15kV/ μs , $V_{DD}\leq 400\text{V}$, $V_{peak}\leq BV_{DSS}$, $T_{ch}\leq 150^\circ\text{C}$.

■ Electrical Characteristics at $T_c=25^\circ\text{C}$ (unless otherwise specified)

• Static Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$ $V_{GS}=0\text{V}$	600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$ $V_{DS}=V_{GS}$	2.5	3.0	3.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=600\text{V}$ $V_{GS}=0\text{V}$ $T_{ch}=25^\circ\text{C}$	-	-	25	μA
		$V_{DS}=480\text{V}$ $V_{GS}=0\text{V}$ $T_{ch}=125^\circ\text{C}$	-	-	250	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}$ $V_{DS}=0\text{V}$	-	10	100	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$I_D=5\text{A}$ $V_{GS}=10\text{V}$	-	0.324	0.38	Ω
Gate resistance	R_G	f=1MHz, open drain	-	3.2	-	Ω

• Dynamic Ratings

Description	Symbol	Conditions	min.	typ.	max.	Unit
Forward Transconductance	g_{fs}	$I_D=5A$ $V_{DS}=25V$	4.5	9.5	-	S
Input Capacitance	C_{iss}	$V_{DS}=10V$	-	760	-	pF
Output Capacitance	C_{oss}	$V_{GS}=0V$	-	1630	-	
Reverse Transfer Capacitance	C_{rss}	$f=1MHz$	-	145	-	
Effective output capacitance, energy related (Note *6)	$C_{o(er)}$	$V_{GS}=0V$ $V_{DS}=0...480V$	-	55	-	
Effective output capacitance, time related (Note *7)	$C_{o(tr)}$	$V_{GS}=0V$ $V_{DS}=0...480V$ $I_D=constant$	-	165	-	
Turn-On Time	$t_{d(on)}$	$V_{DD}=400V, V_{GS}=10V/0V$ $I_D=5A, R_G=27\Omega$ See Fig.3 and Fig.4	-	11	-	ns
	t_r		-	33	-	
Turn-Off Time	$t_{d(off)}$		-	83	-	
	t_f		-	17	-	
Total Gate Charge	Q_G	$V_{DD}=480V, I_D=10A$ $V_{GS}=10V$ See Fig.5	-	28	-	nC
Gate-Source Charge	Q_{GS}		-	8.5	-	
Gate-Drain Charge	Q_{GD}		-	7.5	-	
Drain-Source crossover Charge	Q_{SW}		-	5.5	-	

Note *6 : $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS} .

Note *7 : $C_{o(tr)}$ is a fixed capacitance that gives the same charging times as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS} .

• Reverse Diode

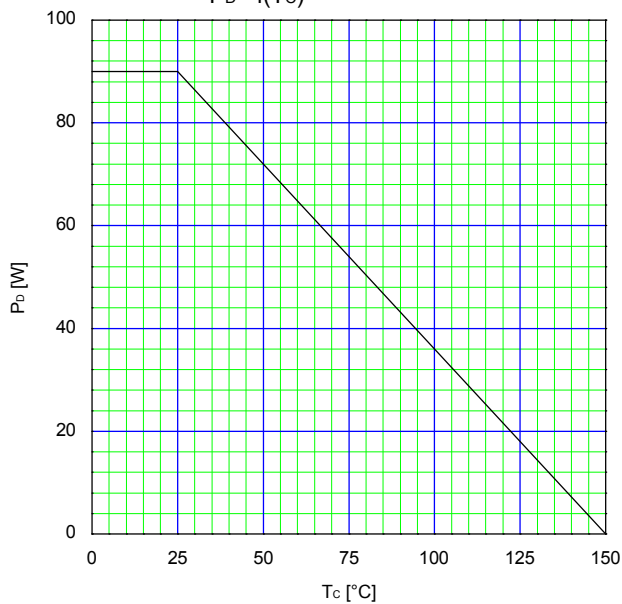
Description	Symbol	Conditions	min.	typ.	max.	Unit
Avalanche Capability	I_{AV}	$L=43.3mH, T_{ch}=25^\circ C$ See Fig.1 and Fig.2	2.9	-	-	A
Diode Forward On-Voltage	V_{SD}	$I_F=10A, V_{GS}=0V$ $T_{ch}=25^\circ C$	-	0.9	1.35	V
Reverse Recovery Time	t_{rr}	$I_F=10A, V_{DD}=400V$ $-di/dt=100A/\mu s$		310	-	ns
Reverse Recovery Charge	Q_{rr}	$V_{GS(Q1)}=short, V_{GS(Q2)}=10V/0V$ $R_G=330\Omega$ $T_{ch}=25^\circ C$	-	3.7	-	μC
Peak Reverse Recovery Current	I_{rp}	See Fig.6 and Fig.7	-	21	-	A

■ Thermal Resistance

Parameter	Symbol	min.	typ.	max.	Unit
Channel to Case	$R_{th(ch-c)}$	-	-	1.39	$^\circ C/W$
Channel to Ambient	$R_{th(ch-a)}$	-	-	62	$^\circ C/W$

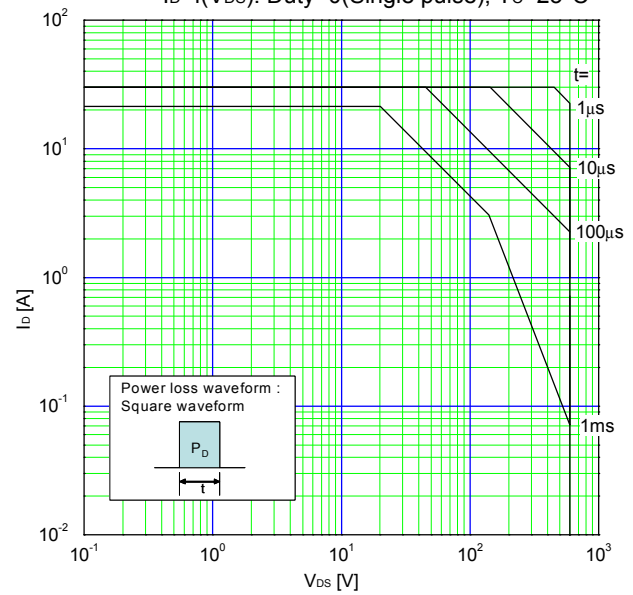
Allowable Power Dissipation

$P_D = f(T_C)$



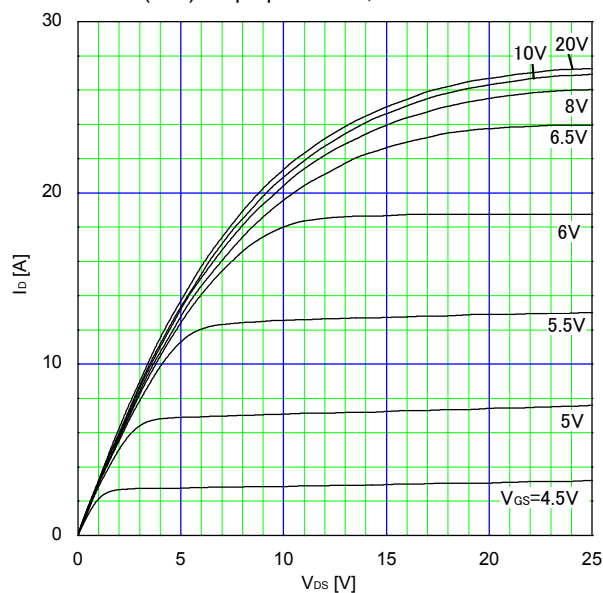
Safe Operating Area

$I_D = f(V_{DS})$; Duty=0 (Single pulse), $T_C = 25^\circ\text{C}$



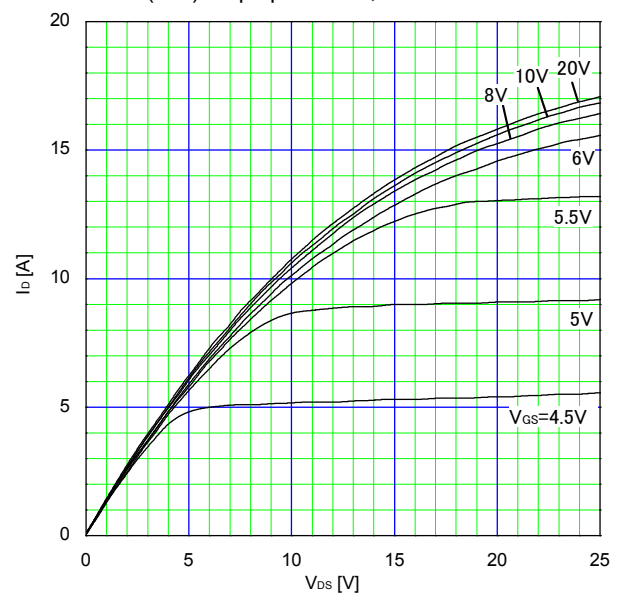
Typical Output Characteristics

$I_D = f(V_{DS})$; 80 μs pulse test, $T_{ch} = 25^\circ\text{C}$



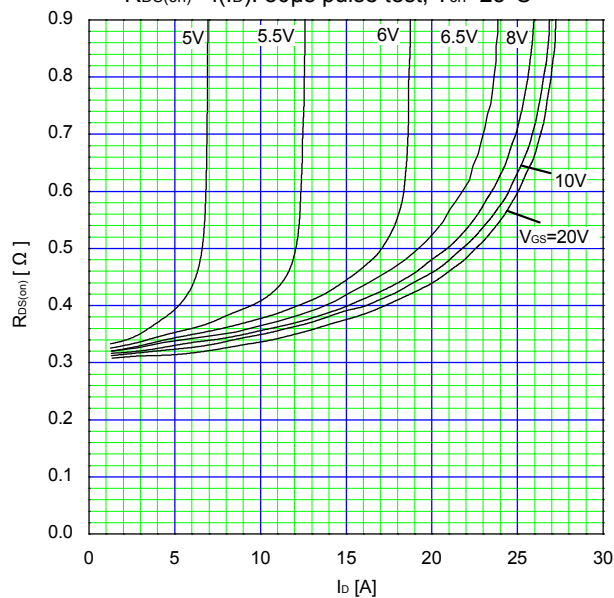
Typical Output Characteristics

$I_D = f(V_{DS})$; 80 μs pulse test, $T_{ch} = 150^\circ\text{C}$



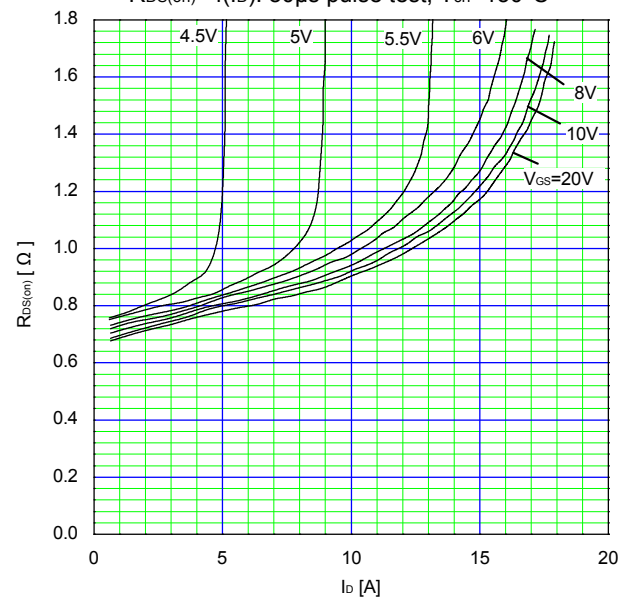
Typical Drain-Source on-state Resistance

$R_{DS(on)} = f(I_D)$; 80 μs pulse test, $T_{ch} = 25^\circ\text{C}$



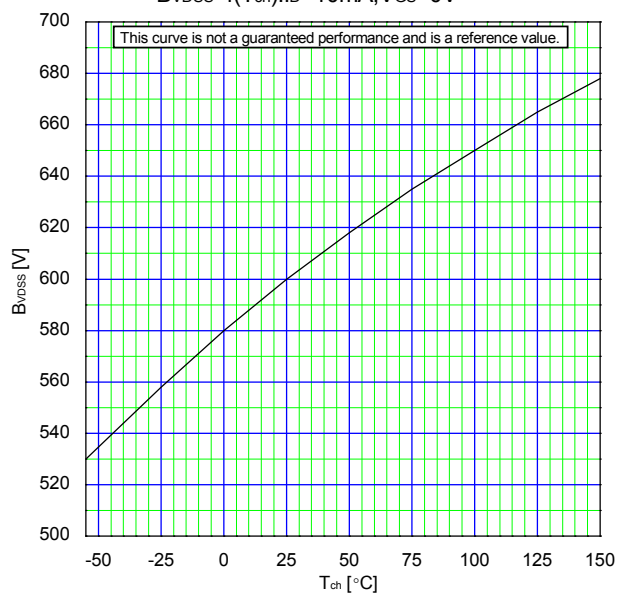
Typical Drain-Source on-state Resistance

$R_{DS(on)} = f(I_D)$; 80 μs pulse test, $T_{ch} = 150^\circ\text{C}$



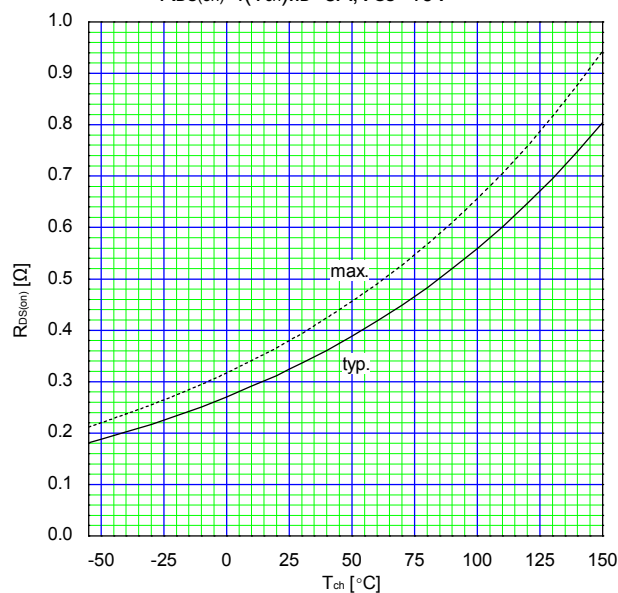
Drain-Source Breakdown Voltage

$$B_{VDS} = f(T_{ch}): I_D = 10\text{mA}, V_{GS} = 0\text{V}$$

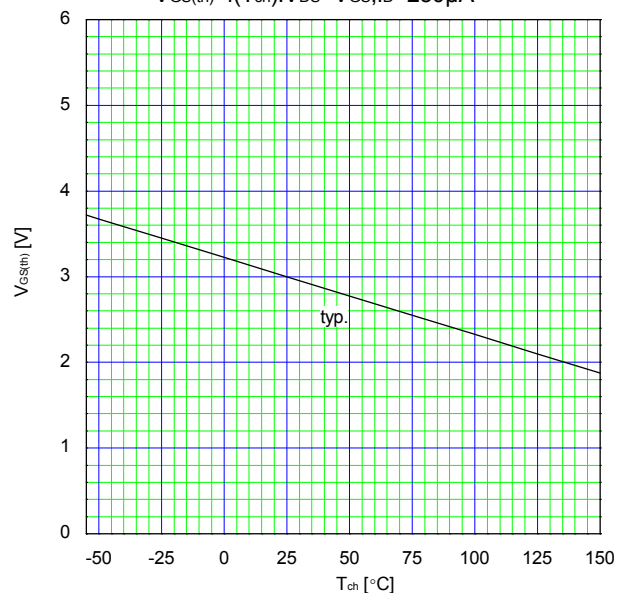


Drain-Source On-state Resistance

$$R_{DS(on)} = f(T_{ch}): I_D = 5\text{A}, V_{GS} = 10\text{V}$$

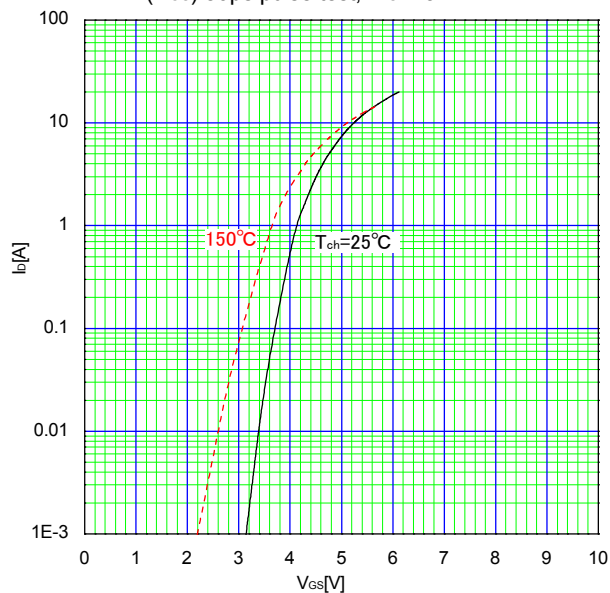
Gate Threshold Voltage vs. T_{ch}

$$V_{GS(th)} = f(T_{ch}): V_{DS} = V_{GS}, I_D = 250\mu\text{A}$$



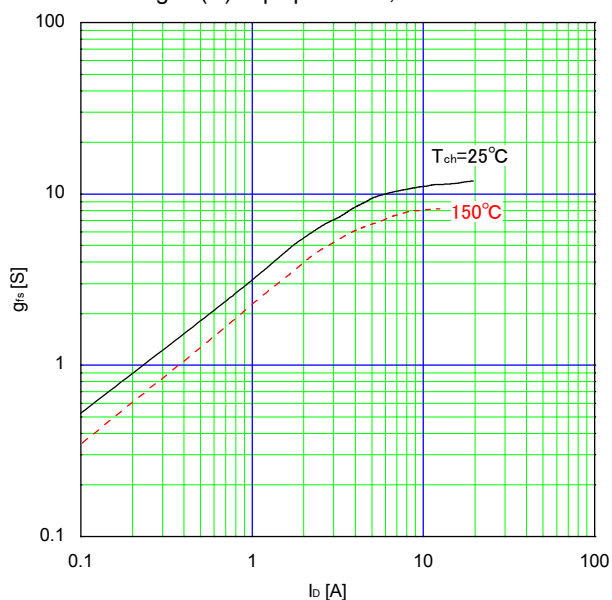
Typical Transfer Characteristic

$$I_D = f(V_{GS}): 80\mu\text{s pulse test}, V_{DS} = 25\text{V}$$



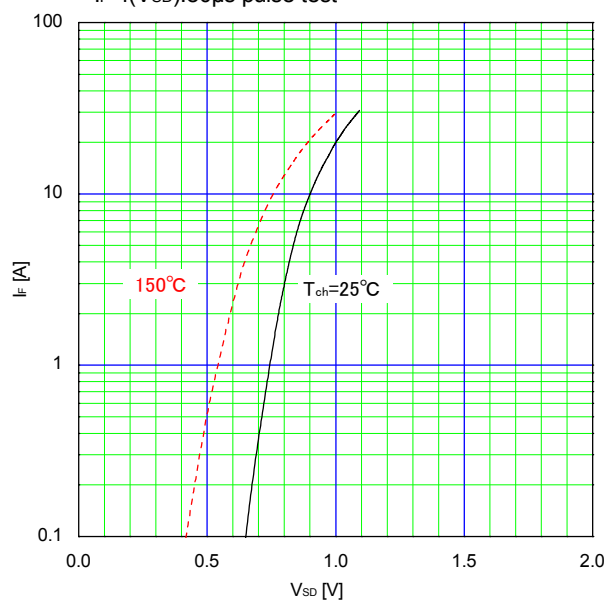
Typical Transconductance

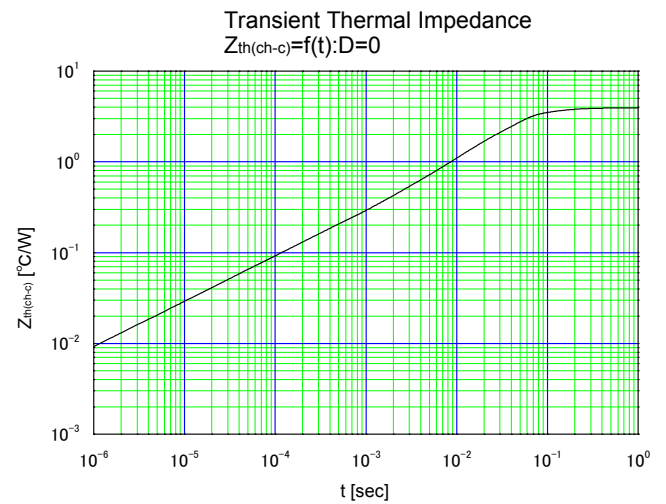
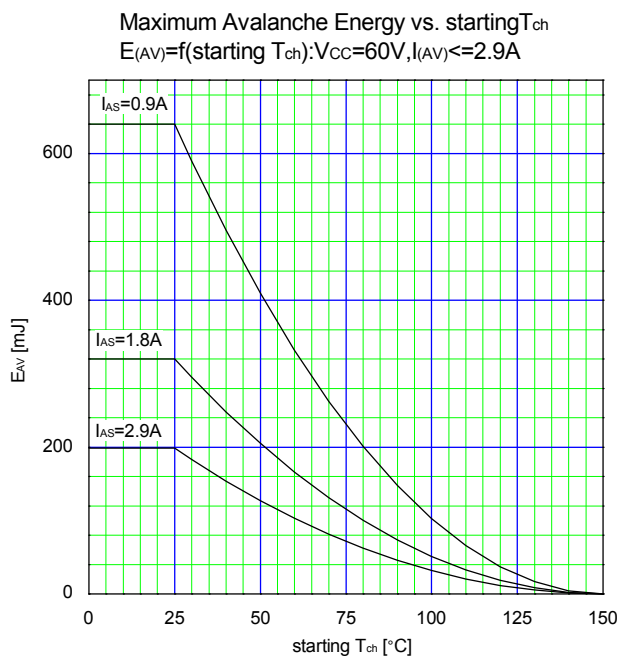
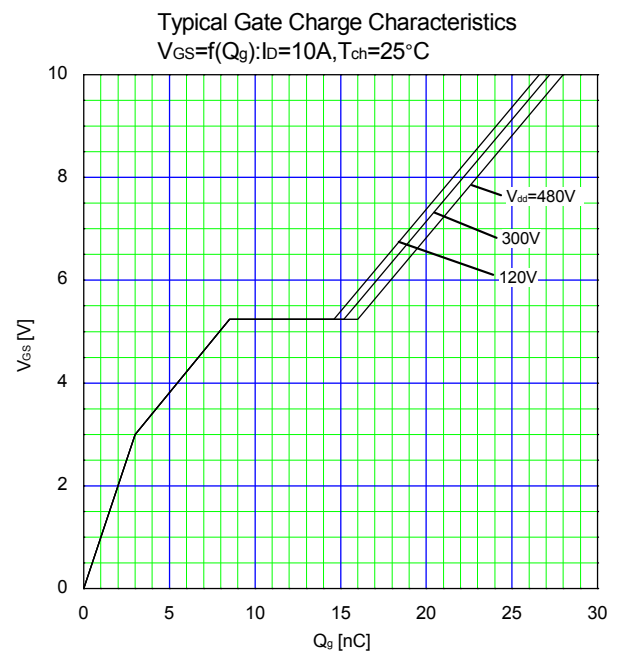
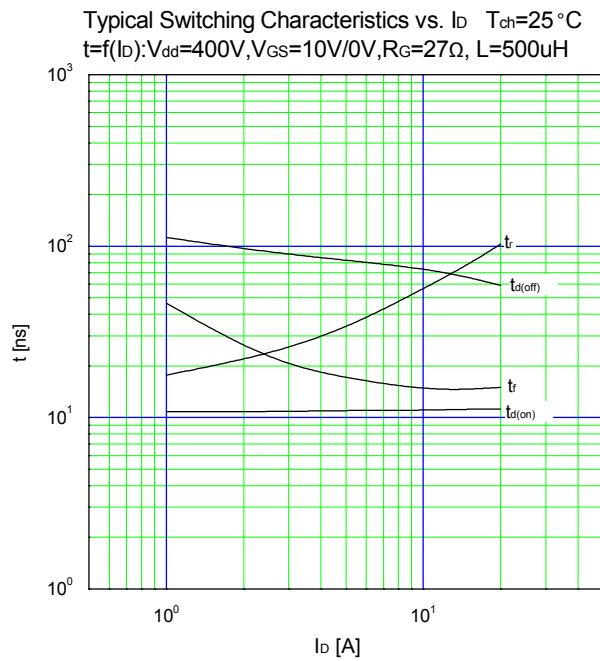
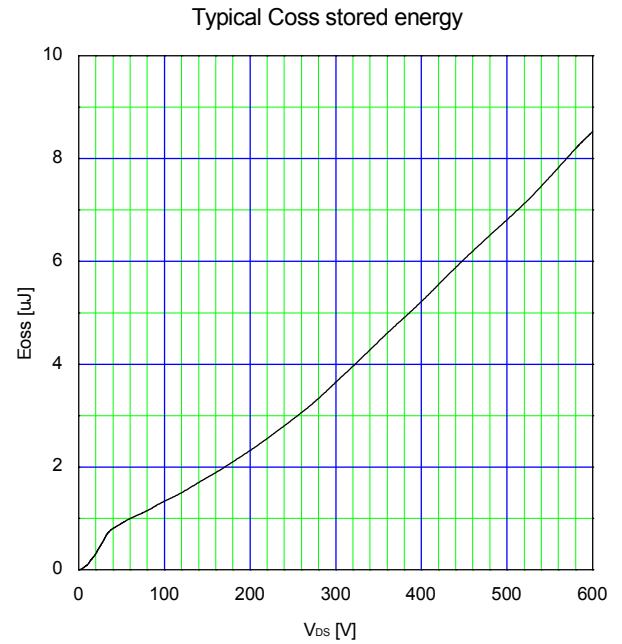
$$g_{fs} = f(I_D): 80\mu\text{s pulse test}, V_{DS} = 25\text{V}$$



Typical Forward Characteristics of Reverse Diode

$$I_F = f(V_{SD}): 80\mu\text{s pulse test}$$





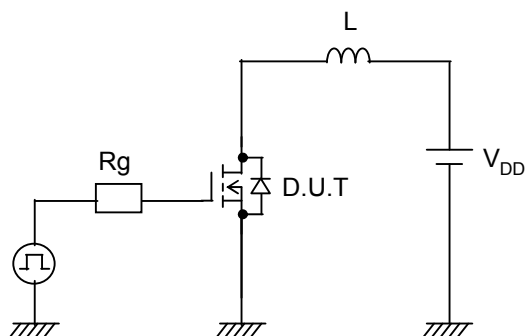


Fig.1 Avalanche Test circuit

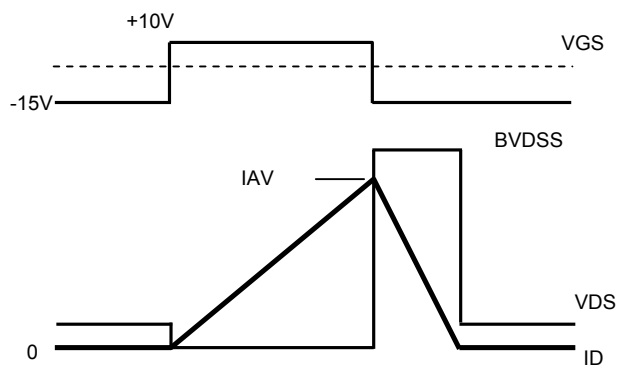


Fig.2 Operating waveforms of Avalanche Test

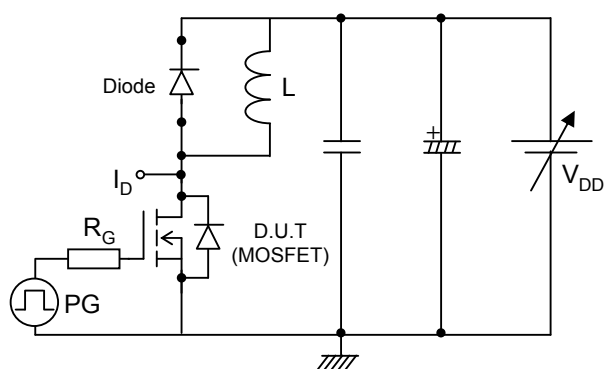


Fig.3 Switching Test circuit

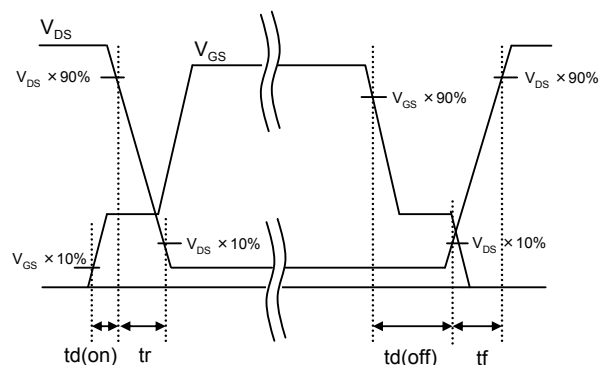


Fig.4 Operating waveform of Switching Test

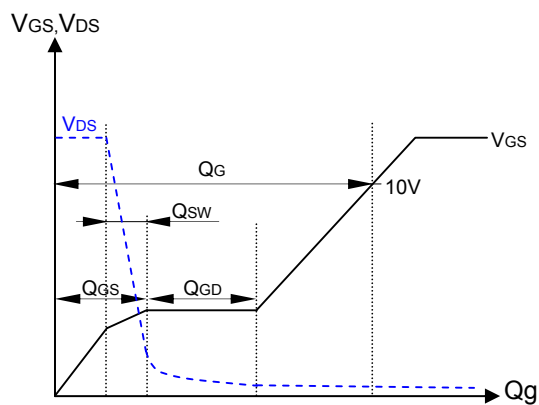


Fig.5 Operating waveform of Gate charge Test

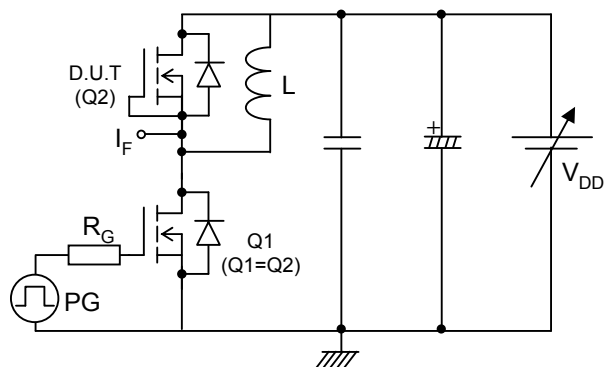


Fig.6 Reverse recovery Test circuit

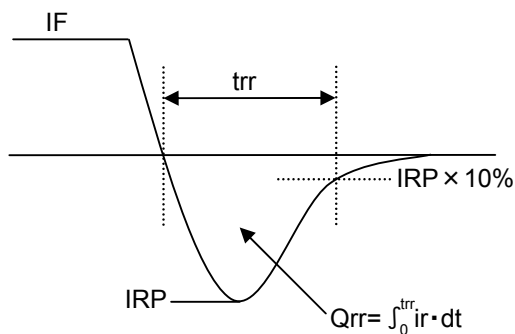
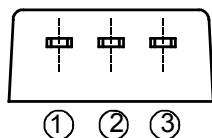
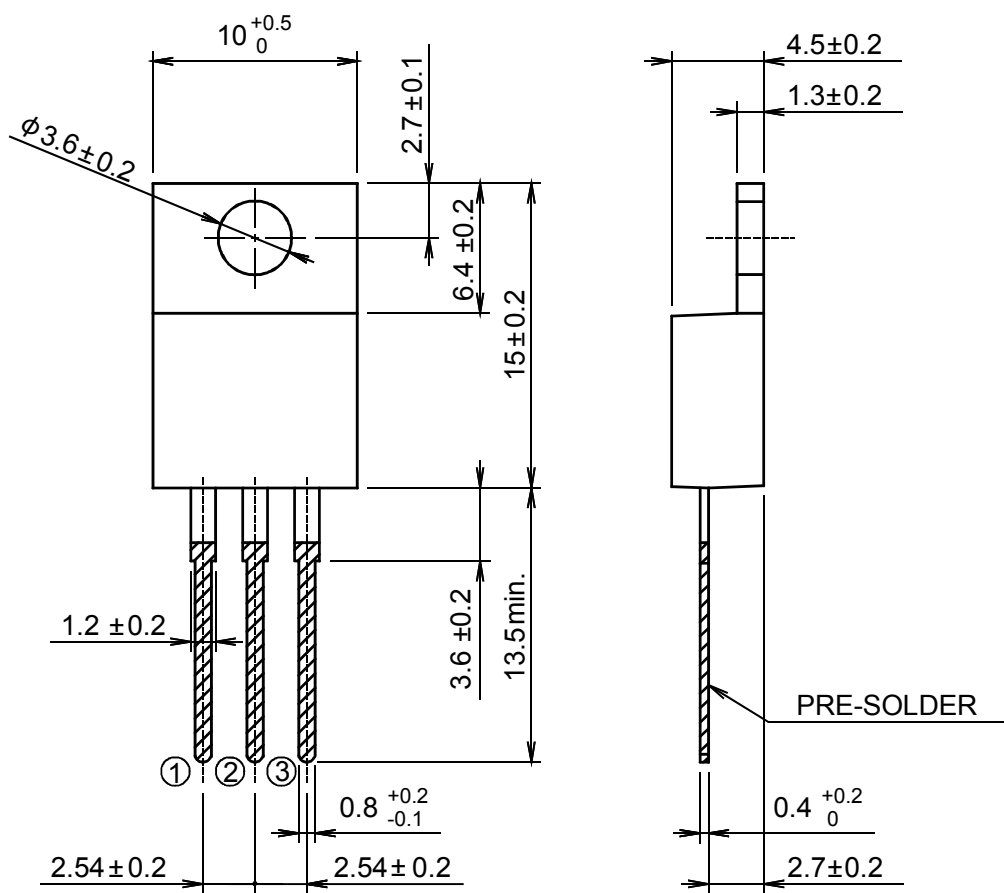


Fig.7 Operating waveform of Reverse recovery Test

■ Outview: TO-220 Package



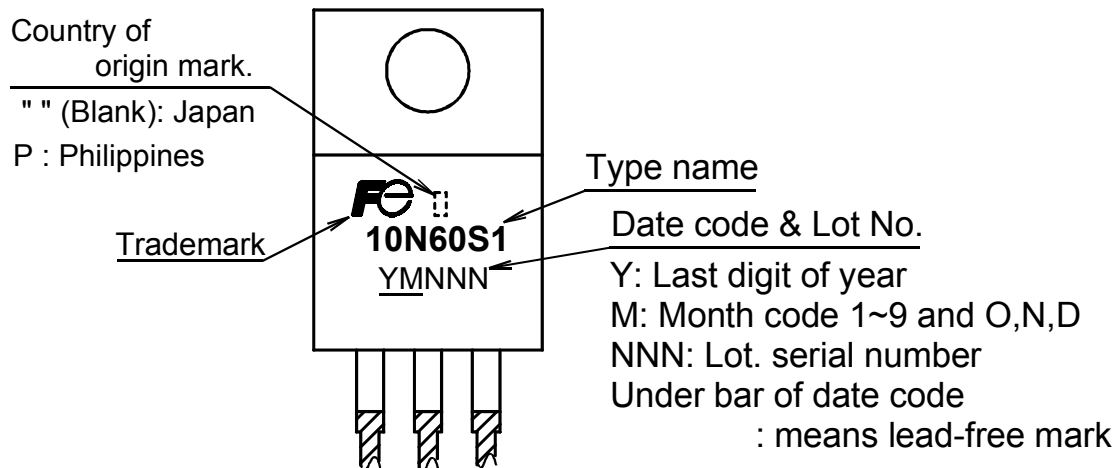
CONNECTION

- ① GATE
- ② DRAIN
- ③ SOURCE

JEDEC : TO-220AB

DIMENSIONS ARE IN MILLIMETERS.

■ Marking



* The font (font type,size) and the trademark-size might be actually different.

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